Hi-performance Regulator IC Series for PCs

Main Power Supply ICs for Note PC (Linear Regulator Integrated)

BD9528MUV

No.10030EAT26

●Description

BD9528MUV is a 2ch switching regulator controller with high output current which can achieve low output voltage (1.0V～5.5V) from a wide input voltage range (5.5V～28V). High efficiency for the switching regulator can be realized by utilizing an external N-MOSFET power transistor. A new technology called H3RegTM(High speed, High efficiency, High performance) is a Rohm proprietary control method to realize ultra high transient response against load change. SLLM (Simple Light Load Mode) technology is also integrated to improve efficiency in light load mode, providing high efficiency over a wide load range. For protection and ease of use, 2ch LDO (5V/100mA, 3.3V/100mA), the soft start function, variable frequency function, short circuit protection function with timer latch, over voltage protection, and Power good function are all built in. This switching regulator is specially designed for Main Power Supply of laptop PC.

●Features

1) 2ch H^3REG^{TM} DC/DC Converter controller
2) Adjustable Simple Light Load Mode (SLLM), Quiet Light Load Mode (QLLM) and Forced continuous Mode
3) Thermal Shut Down (TSD), Under Voltage LockOut (UVLO), Over Current Protection (OCP), Over Voltage Protection (OVP), Short circuit protection with 0.75ms timer-latch (SCP)
4) Soft start function to minimize rush current during startup
5) Switching Frequency Variable (f=200kHz～500kHz)
6) Built-in Power good circuit
7) Built-in 2ch Linear regulator (5V/100mA,3.3V/100mA)
8) Built in reference voltage(0.7V)
9) VQFN032V5050 package
10) Built-in BOOT-Di
11) Built-in output discharge

●Applications

Laptop PC, Desktop PC, LCD-TV, Digital Components

●**Absolute maximum ratings** (Ta=25℃)

Parameter	Symbol	Limits	Unit
Terminal Voltage	VIN, CTL,SW1,SW2	30 *1*2	V
	EN1, EN2, PGOOD1, PGOOD2 Vo1, Vo2, MCTL1, MCTL2	6 *1*2	V
	FS1, FS2, FB1, FB2, ILIM1, ILIM2, SS1, SS2, LG1, LG2, REF,REG2	REG1+0.3 *1	V
	BOOT1, BOOT2	35 *1*2	V
	BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2	7 *1*2	V
	HG1	BOOT1+0.3 *1*2	V
	HG2	BOOT2+0.3 *1*2	V
	PGND1, PGND2	AGND±0.3 *1*2	V
Power Dissipation1	Pd1	0.38 *3	W
Power Dissipation2	Pd2	0.88 *4	W
Power Dissipation3	Pd3	3.26 *5	W
Power Dissipation4	Pd4	4.56 *6	W
Operating temperature Range	Topr	-20～+100	℃
Storage temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	+150	℃

*1 Do not however exceed Pd.
*2 Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
*3 Reduced by 3.0mW for each increase in Ta of 1℃ over 25℃ (when don't mounted on a heat radiation board)
*4 Reduced by 7.0mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 74.2mm × 74.2mm × 1.6mm Glass-epoxy PCB which has 1 layer. (Copper foil area : 20.2mm^2)
*5 Reduced by 26.1mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 74.2mm × 74.2mm × 1.6mm Glass-epoxy PCB which has 4 layers. (1st and 4th copper foil area : 20.2mm^2, 2nd and 3rd copper foil area : 5505mm^2)
*6 Reduced by 36.5mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 74.2mm × 74.2mm × 1.6mm Glass-epoxy PCB which has 4 layers. (All copper foil area : 5505mm^2)

●**Operating conditions**(Ta=25℃)

Parameter	Symbol	MIN.	MAX.	Unit
Terminal Voltage	VIN	5.5	28	V
	CTL	-0.3	28	V
	EN1, EN2, MCTL1, MCTL2	-0.3	5.5	V
	BOOT1, BOOT2	4.5	33	V
	SW1, SW2	-0.3	28	V
	BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2	-0.3	5.5	V
	Vo1, Vo2, PGOOD1, PGOOD2	-0.3	5.5	V
MIN ON TIME	TONmin	-	150	nsec

★ This product should not be used in a radioactive environment.

●**Electrical characteristics**

(unless otherwise noted, Ta=25℃ VIN=12V, CTL=OPEN, EN1=EN2=5V, FS1=FS2=51kΩ)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN.	TYP.	MAX.		
VIN standby current	ISTB	70	150	250	μA	CTL=5V, EN1=EN2=0V
VIN bias current	IIN	60	130	230	μA	Vo1=5V
VIN shut down mode current	ISHD	6	12	18	μA	CTL=0V
CTL Low Voltage	VCTLL	-0.3	-	0.8	V	
CTL High Voltage	VCTLH	2.3	-	28	V	
CTL bias current	ICTL	-18	-12	-6	μA	CTL=0V
EN Low Voltage	VENL	-0.3	-	0.8	V	
EN High Voltage	VENH	2.3	-	5.5	V	
EN bias current	IEN	-	3	6	μA	EN=3V
[5V linear regulator](VIN)						
REG1 output voltage	VREG1	4.90	5.00	5.10	V	IREG1=1mA
Maximum current	IREG1	100	-	-	mA	IREG2=0mA
Line Regulation	Reg.l1	-	90	180	mV	VIN=5.5 to 25V
Load Regulation	Reg.L1	-	30	50	mV	IREG1=0 to 30mA
[3.3V linear regulator]						
REG2 output voltage	VREG2	3.27	3.30	3.33	V	IREG2=1mA
Maximum current	IREG2	100	-	-	mA	IREG1=0mA
Line Regulation	Reg.l2	-	-	20	mV	VIN=5.5 to 25V
Load Regulation	Reg.L2	-	-	30	mV	IREG2=0 to 30mA
[5V linear regulator](Vo1)						
Input threshold voltage	REG1th	4.1	4.4	4.7	V	Vo1: Sweep up
Input delay time	TREG1	1.5	3.0	6.0	ms	
Switch resistance	RREG1	-	1.0	3.0	Ω	
[Under Voltage lock out block]						
REG1 threshold voltage	REG1_UVLO	3.9	4.2	4.5	V	REG1: Sweep up
Hysteresis voltage	dV_UVLO	50	100	200	mV	REG1, Sweep down
[Output voltage sense block]						
Feedback voltage1	VFB1	0.693	0.700	0.707	V	
FB1 bias current	IFB1	-	0	1	μA	FB1=REF
Output discharge resistance1	RDISOUT1	50	100	200	Ω	
Feedback voltage2	VFB2	0.693	0.700	0.707	V	
FB2 bias current	IFB2	-	0	1	μA	FB2=REF
Output discharge resistance2	RDISOUT2	50	100	200	Ω	

●**Electrical characteristics – Continued**

(unless otherwise noted, Ta=25℃ VIN=12V, CTL=OPEN, EN1=EN2=5V, FS1=FS2=51kΩ)

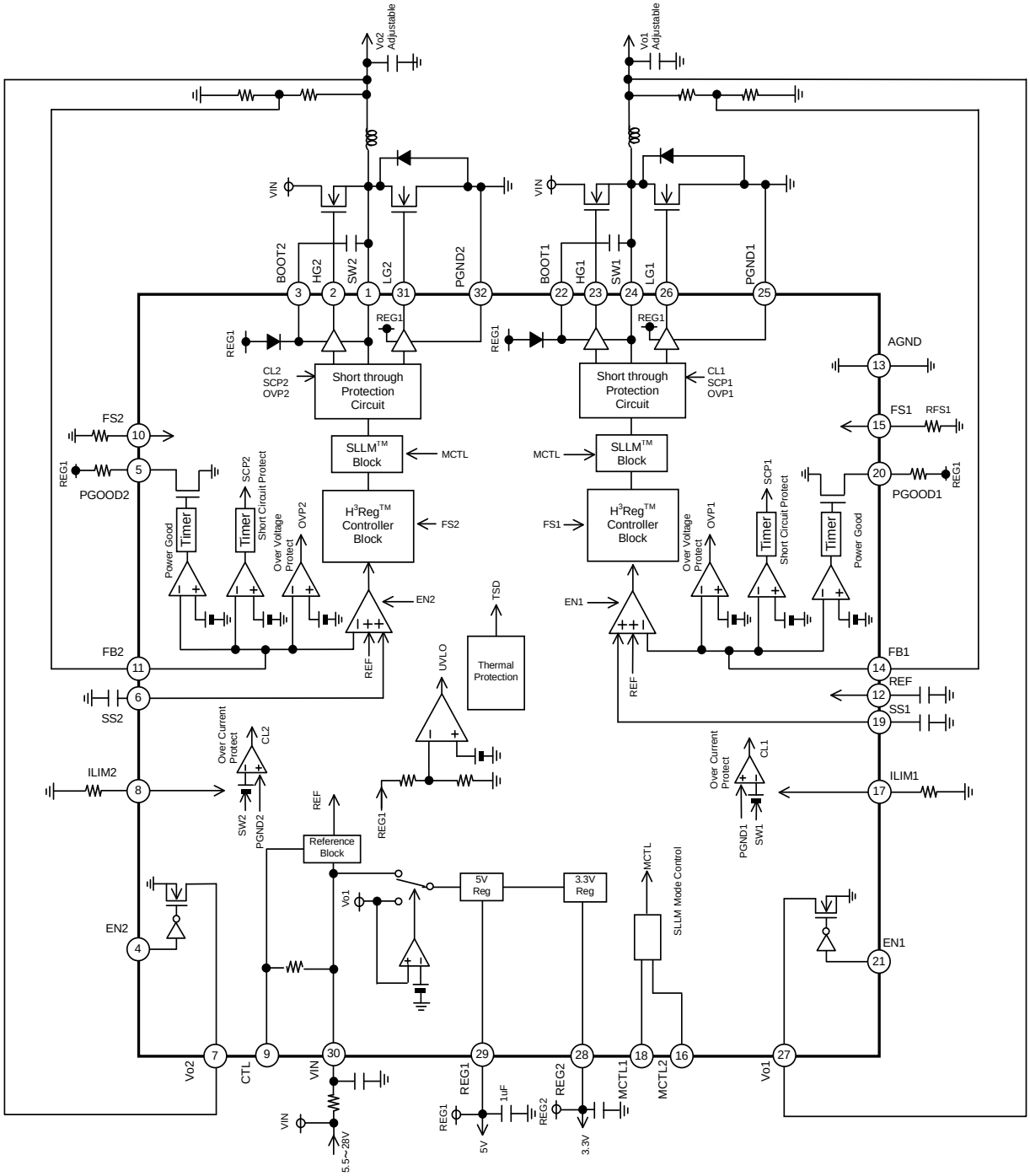
Parameter	Symbol	Standard Value			Unit	Condition
		MIN.	TYP.	MAX.		
[H^{3}REG block]						
Ontime1	TON1	0.760	0.910	1.060	μs	Vo1=5V
Ontime2	TON2	0.470	0.620	0.770	μs	Vo2=3.3V
Maximum On time 1	TONMAX1	2.5	5	10	μs	Vo1=5V
Maximum On time 2	TONMAX2	1.65	3.3	6.6	μs	Vo2=33V
Minimum Off time	TOFFMIN	-	0.2	0.4	μs	
[FET driver block]						
HG higher side ON resistor	HGHON	-	3.0	6.0	Ω	
HG lower side ON resistor	HGLON	-	2.0	4.0	Ω	
LG higher side ON resistor	LGHON	-	2.0	4.0	Ω	
LG lower side ON resistor	LGLON	-	0.5	1.0	Ω	
[Over voltage protection block]						
OVP threshold voltage	VOVP	0.77 (+10%)	0.84 (+20%)	0.91 (+30%)	V	
OVP Hysteresis	dV_OVP	50	150	300	mV	
[Short circuit protection block]						
SCP threshold voltage	VSCP	0.42 (-40%)	0.49 (-30%)	0.56 (-20%)	V	
Delay time	TSCP	0.4	0.75	1.5	ms	
[Current limit protection block]						
Offset voltage	dVSMAX	80	100	120	mV	ILIM=100kΩ
[Power good block]						
Power good low threshold	VPGTHL	0.525 (-25%)	0.595 (-15%)	0.665 (-5%)	V	
Power good low voltage	VPGL	-	0.1	0.2	V	IPGOOD=1mA
Delay time	TPGOOD	0.4	0.75	1.5	ms	
Power good leakage current	ILEAKPG	-2	0	2	μA	VPGOOD=5V
[Soft start block]						
Charge current	ISS	1.5	2.3	3.1	μA	
Standby voltage	VSS_STB	-	-	50	mV	
[Mode control block]						
MCTL Low voltage	VMCTL_L	-0.3	-	0.3	V	
MCTL High voltage	VMCTL_H	2.3	-	REG1 +0.3	V	
MCTL bias current	IMCTL	8	16	24	μA	MCTL=5V

●Output condition table

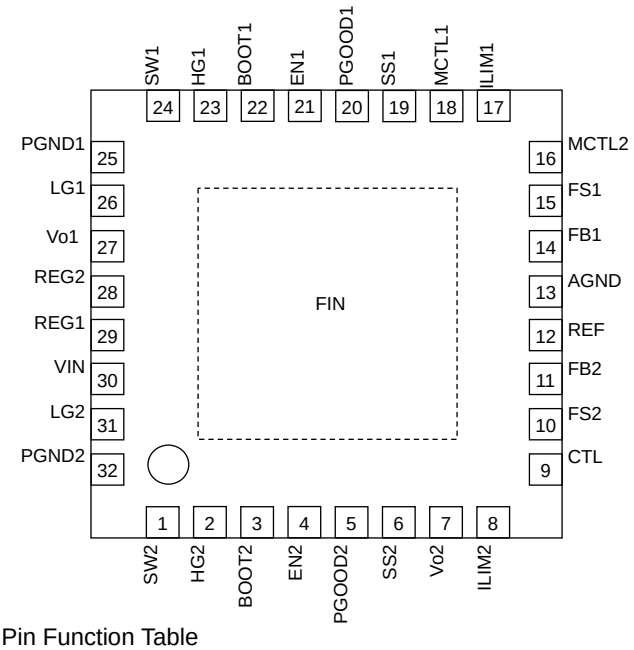
Input			Output			
CTL	EN1	EN2	REG1(5V)	REG2(3.3V)	DC/DC1	DC/DC2
Low	Low	Low	OFF	OFF	OFF	OFF
Low	Low	High	OFF	OFF	OFF	OFF
Low	High	Low	OFF	OFF	OFF	OFF
Low	High	High	OFF	OFF	OFF	OFF
High	Low	Low	ON	ON	OFF	OFF
High	Low	High	ON	ON	OFF	ON
High	High	Low	ON	ON	ON	OFF
High	High	High	ON	ON	ON	ON

※ CTL pin is connected to VIN pin with 1MΩ resistor(pull up) internal IC.
※ EN pin is connected to AGND pin with 1MΩ resistor(pull down) internal IC.

●Block Diagram, Application circuit



●Pin Configuration



Input		Control Mode
MCTL1	MCTL2	
Low	Low	SLLM
Low	High	QLLM
High	Low	Forced Continuous Mode
High	High	Forced Continuous Mode

※MCTL pin is connected to AGND pin with 500kΩ resistor (pull down) internal IC

●Pin Function Table

PIN No.	PIN name	PIN Function
1	SW2	Highside FET source pin 2
2	HG2	Highside FET gate drive pin 2
3	BOOT2	HG Driver power supply pin 2
4	EN2	Vo2 ON/OFF pin (High=ON, Low,OPEN=OFF)
5	PGOOD2	Vo2 Power Good Open Drain Output pin
6	SS2	Vo2 Soft start pin
7	Vo2	Vo2 Output voltage sense pin
8	ILIM2	OCP setting pin 2
9	CTL	Linear regulator ON/OFF pin (High,OPEN=ON, Low=OFF)
10	FS2	Input pin for setting Vo2 frequency
11	FB2	Vo2 output voltage feedback pin
12	REF	Output voltage setting pin
13	AGND	Input pin Ground
14	FB1	Vo1 output voltage feedback pin
15	FS1	Input pin for setting Vo1 frequency
16	MCTL2	Mode switch pin 2 (OPEN = L)
17	ILIM1	OCP setting pin 1
18	MCTL1	Mode switch pin 1 (OPEN = L)
19	SS1	Vo1 Soft start pin
20	PGOOD1	Vo1 Power Good Open Drain Output pin
21	EN1	Vo1 ON/OFF pin (High=ON, Low,OPEN=OFF)
22	BOOT1	HG Driver power supply pin
23	HG1	Highside FET gate drive pin 1
24	SW1	Highside FET source pin 1
25	PGND1	Lowside FET source pin 1
26	LG1	Lowside FET gate drive pin 1
27	Vo1	Vo1 Output voltage sense pin
28	REG2	3.3V Linear regulator output pin
29	REG1	5V Linear regulator output pin
30	VIN	Power supply input pin
31	LG2	Lowside FET gate drive pin 2
32	PGND2	Lowside FET source pin 2
reverse	FIN	Exposed Pad1, connect to GND

●Electrical characteristic curves (Reference data)

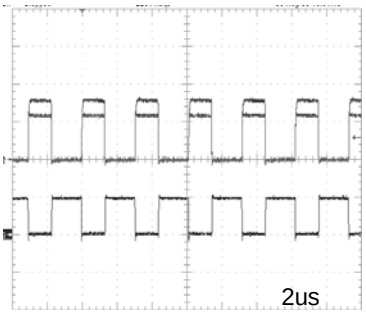


Fig.1 Switching Waveform
(Vo=5V, PWM, Io=0A)

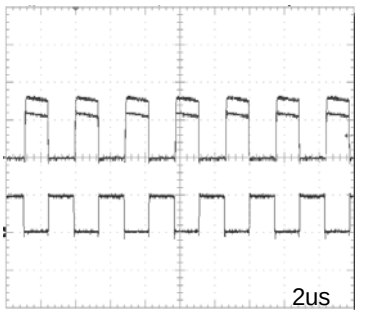


Fig.2 Switching Waveform
(Vo=5V, PWM, Io=8A)

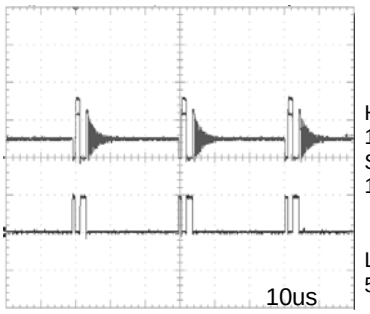


Fig.3 Switching Waveform
(Vo=5V, QLLM, Io=0A)

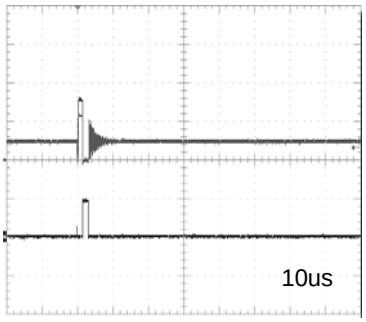


Fig.4 Switching Waveform
(Vo=5V, SLLM, Io=0A)

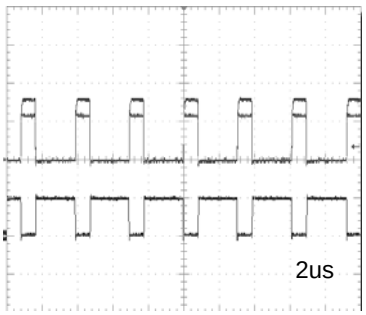


Fig.5 Switching Waveform
(Vo=3.3V, PWM, Io=0A)

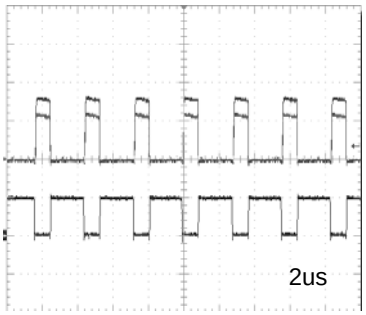


Fig.6 Switching Waveform
(Vo=3.3V, PWM, Io=8A)

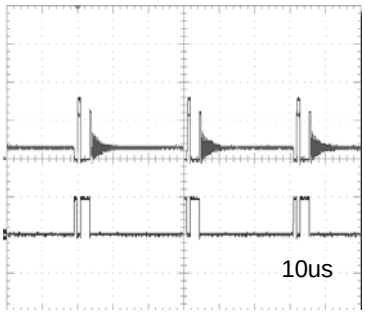


Fig.7 Switching Waveform
(Vo=3.3V, QLLM, Io=0A)

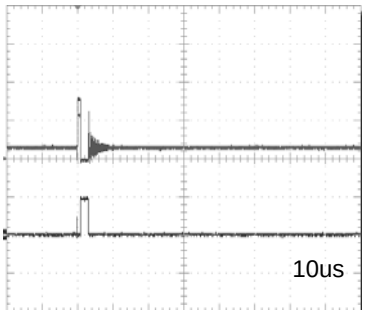


Fig.8 Switching Waveform
(Vo=3.3V, SLLM, Io=0A)

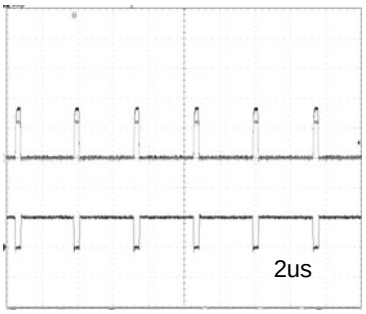


Fig.9 Switching Waveform
(Vo=1V, PWM, Io=0A)

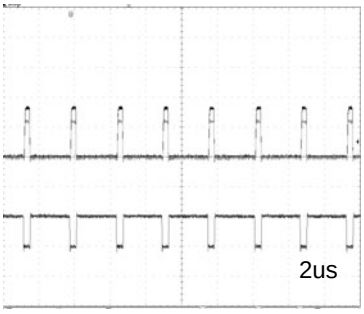


Fig.10 Switching Waveform
(Vo=1V, PWM, Io=8A)

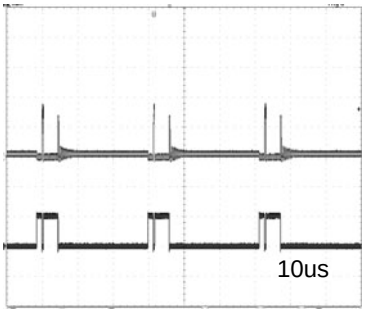


Fig.11 Switching Waveform
(Vo=1V, QLLM, Io=0A)

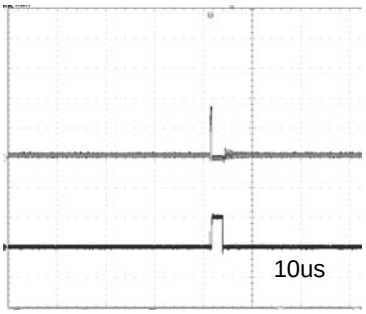


Fig.12 Switching Waveform
(Vo=1V, SLLM, Io=0A)

●Electrical characteristic curves (Reference data) – Continued

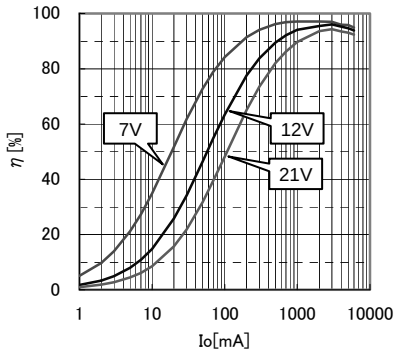


Fig.13 Efficiency
(Vo=5V, PWM)

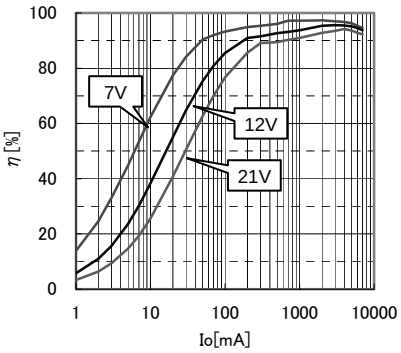


Fig.14 Efficiency
(Vo=5V, QLLM)

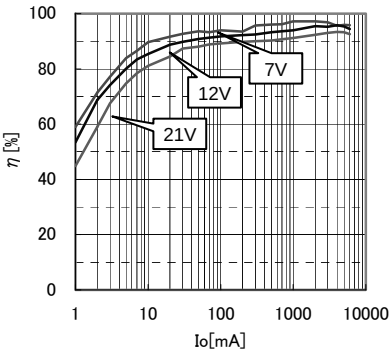


Fig.15 Efficiency
(Vo=5V, SLLM)

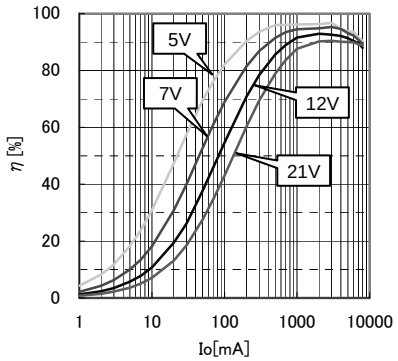


Fig.16 Efficiency
(Vo=3.3V, PWM)

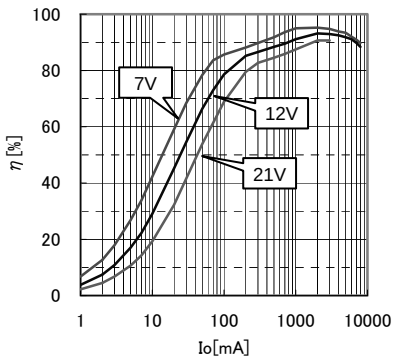


Fig.17 Efficiency
(Vo=3.3V, QLLM)

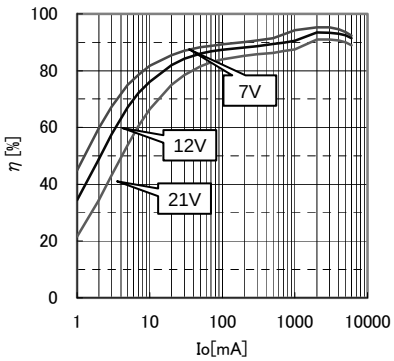


Fig.18 Efficiency
(Vo=3.3V, SLLM)

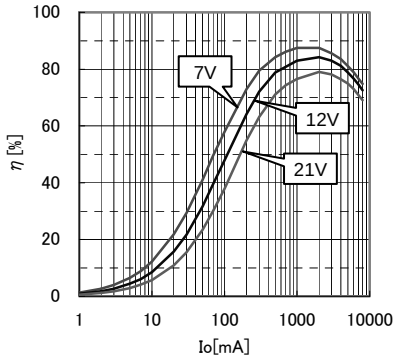


Fig.19 Efficiency
(Vo=1V, PWM)

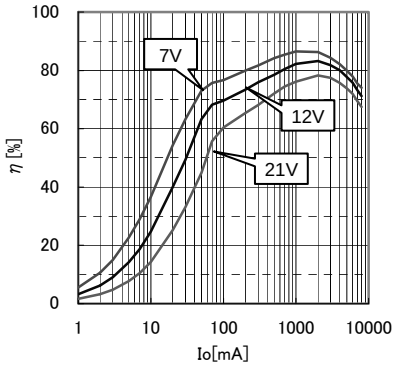


Fig.20 Efficiency
(Vo=1V, QLLM)

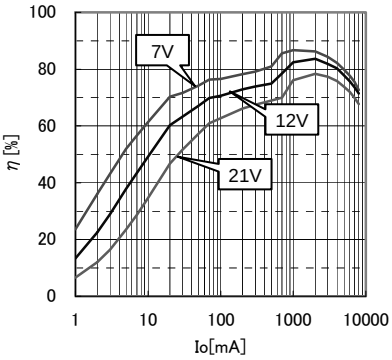


Fig.21 Efficiency
(Vo=1V, SLLM)

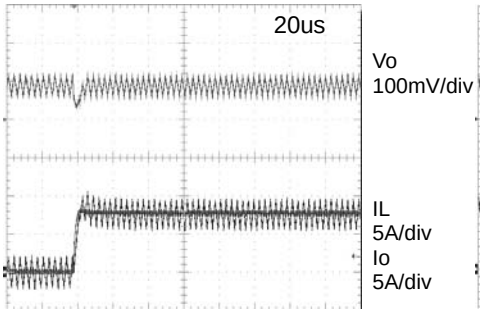


Fig.22 Transient Response
(Vo=5V, PWM, Io=0→8A)

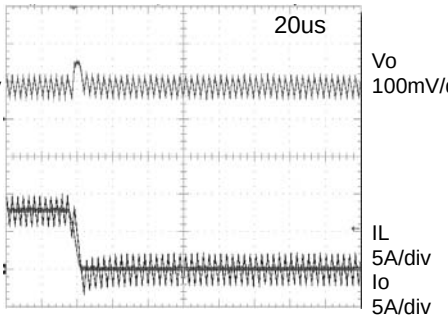


Fig.23 Transient Response
(Vo=5V, PWM, Io=8→0A)

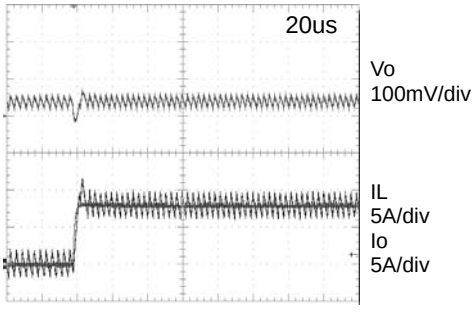


Fig.24 Transient Response
(Vo=3.3V, PWM, Io=0→8A)

●Electrical characteristic curves (Reference data) – Continued

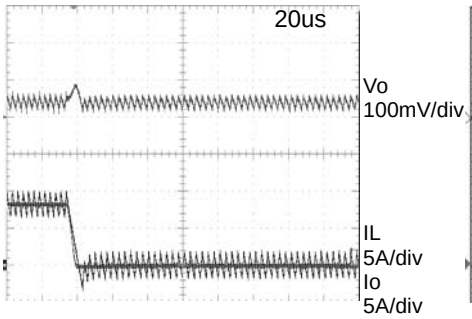


Fig.25 Transient Response
(Vo=3.3V, PWM, Io=8→0A)

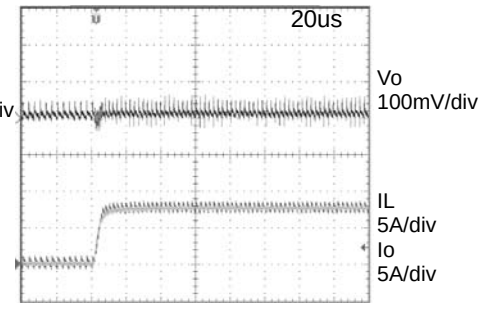


Fig.26 Transient Response
(Vo=1V, PWM, Io=0→8A)

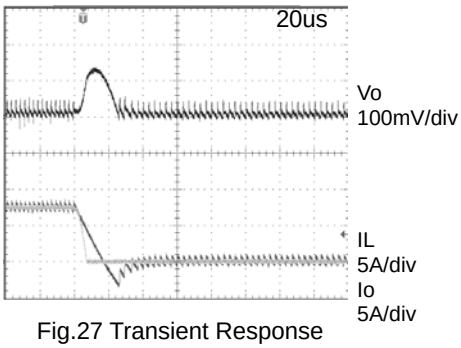


Fig.27 Transient Response
(Vo=1V, PWM, Io=8→0A)

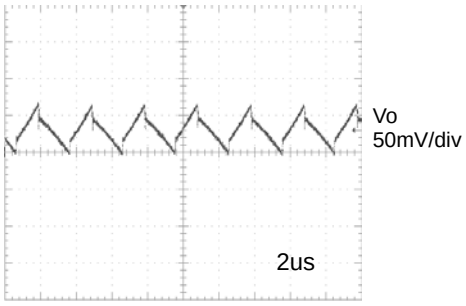


Fig.28 Output Voltage
(Vo=5V, PWM, Io=0A)

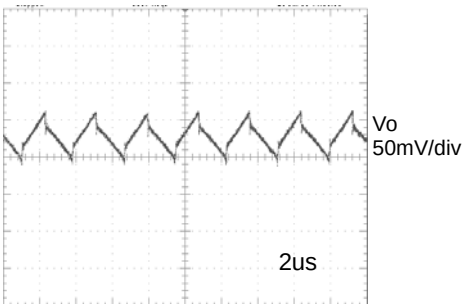


Fig.29 Output Voltage
(Vo=5V, PWM, Io=8A)

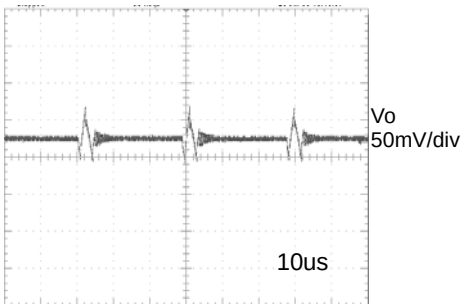


Fig.30 Output Voltage
(Vo=5V, QLLM, Io=0A)

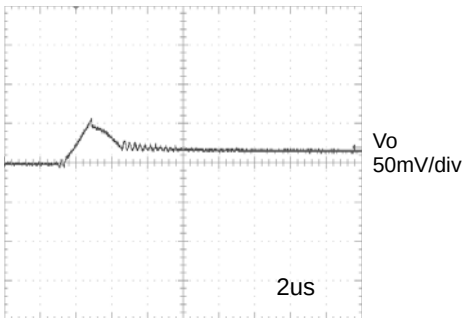


Fig.31 Output Voltage
(Vo=5V, SLLM, Io=0A)

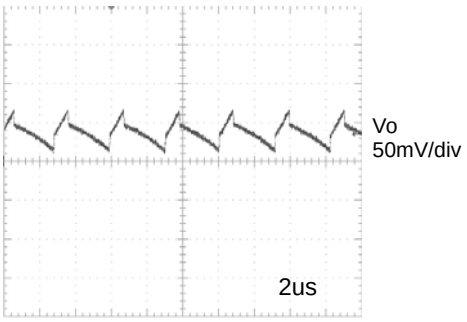


Fig.32 Output Voltage
(Vo=3.3V, PWM, Io=0A)

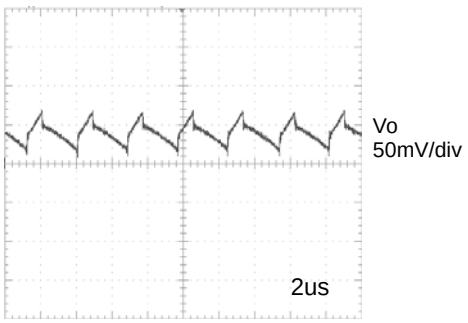


Fig.33 Output Voltage
(Vo=3.3V, PWM, Io=8A)

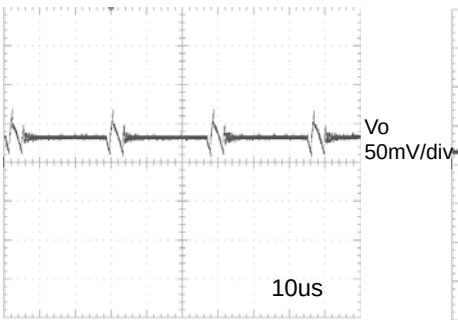


Fig.34 Output Voltage
(Vo=3.3V, QLLM, Io=0A)

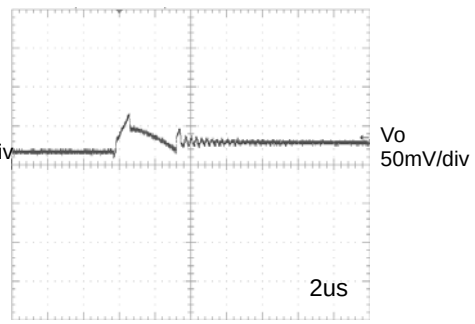


Fig.35 Output Voltage
(Vo=3.3V, SLLM, Io=0A)

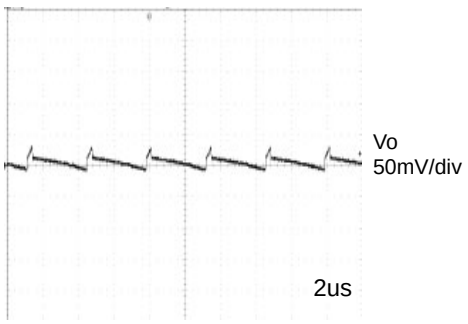


Fig.36 Output Voltage
(Vo=1V, PWM, Io=0A)

●Electrical characteristic curves (Reference data) – Continued

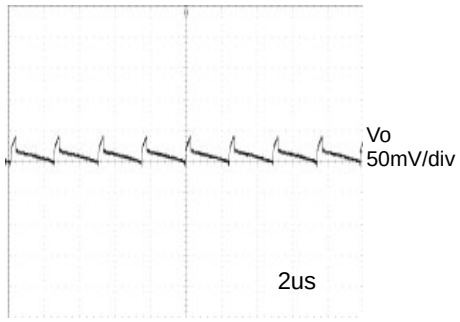


Fig.37 Output Voltage
(Vo=1V, PWM, Io=8A)

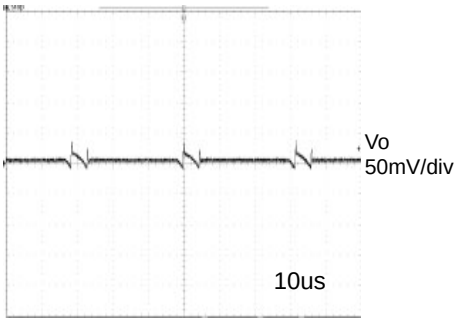


Fig.38 Output Voltage
(Vo=1V, QLLM, Io=0A)

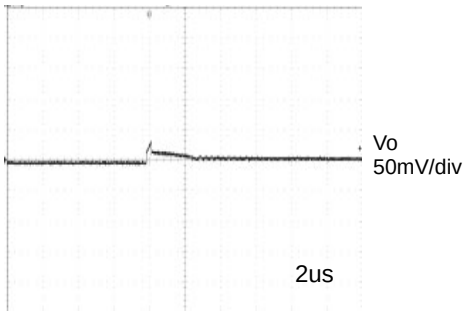


Fig.39 Output Voltage
(Vo=1V, SLLM, Io=0A)

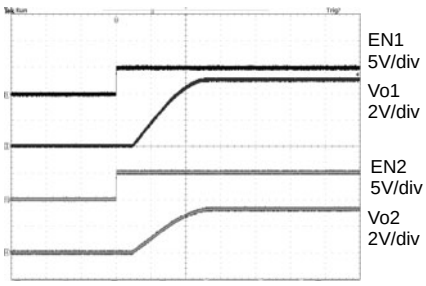


Fig.40 Wake up waveform
(EN1=EN2)

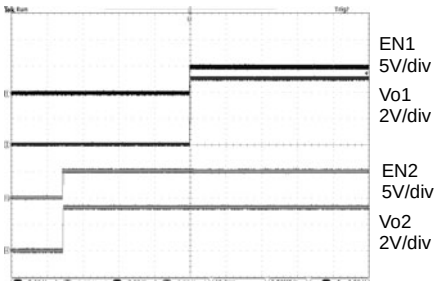


Fig.41 Wake up waveform
(EN2→EN1)

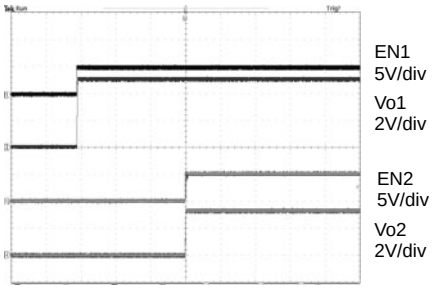


Fig.42Wake up waveform
(EN1→EN2)

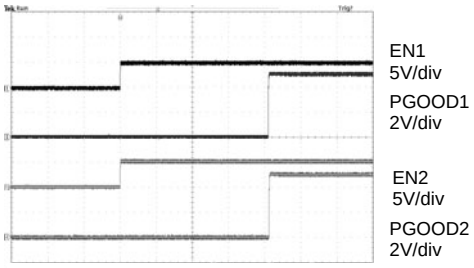


Fig.43Wake up waveform
(EN1/2→PGOOD1/2)

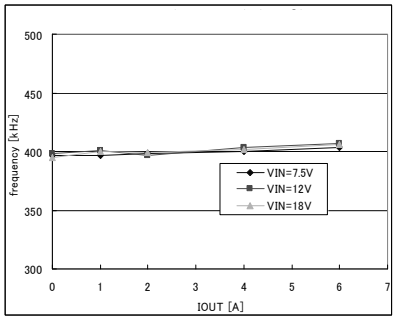


Fig.44 Io-frequency
(Vo=5V, PWM, RFS=68kΩ)

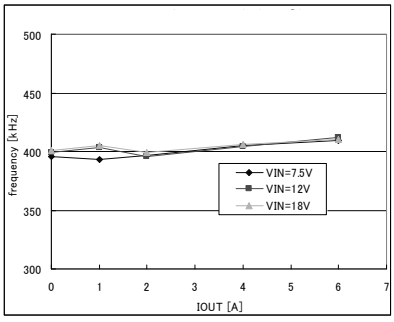


Fig.45 Io-frequency
(Vo=3.3V, PWM, RFS=68kΩ)

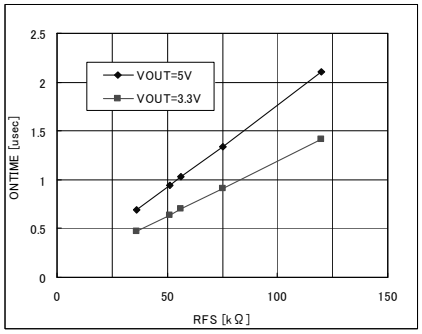


Fig.46 FS-ONTIME

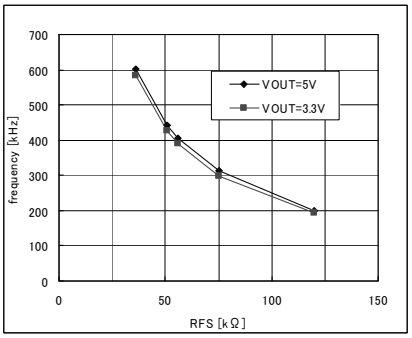


Fig.47 FS-frequency

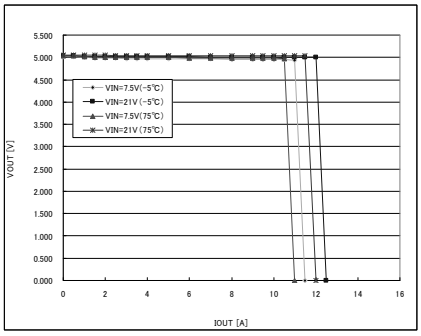


Fig.48 Ta-IOCP
(Vo=5V)

●Electrical characteristic curves (Reference data) – Continued

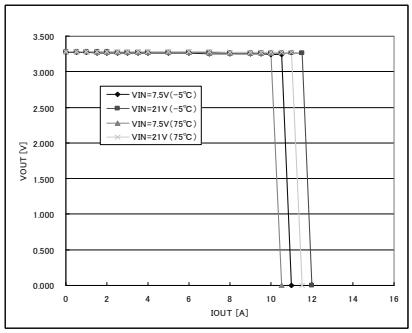


Fig.49 Ta-IOCP
(Vo=3.3V)

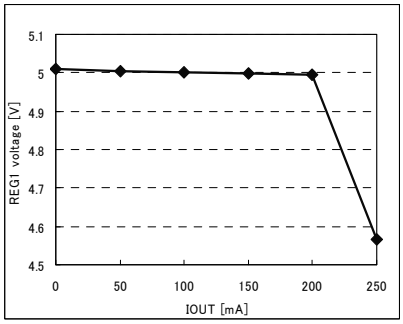


Fig.50 IREG1-REG1

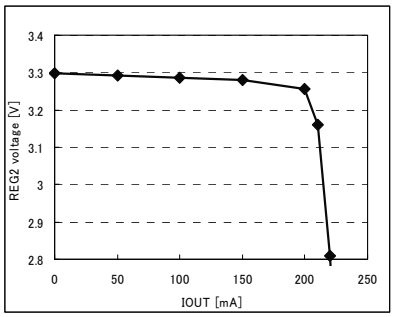


Fig.51 IREG2-REG2

●Pin Descriptions

・VIN (30 pin)
This is the main power supply pin. The input supply voltage range is 5.5V to 25V. The duty cycle of BD9528MUV is determined by input voltage and control output voltage. Therefore, when VIN voltage fluctuated, the output voltage also becomes unstable. Since VIN line is also the input voltage of switching regulator, stability depends on the impedance of the voltage supply. It is recommended to establish bypass capacitor and CR filter suitable for the actual application.

・CTL (9 pin)
When CTL pin voltage is at least 2.3V, the status of the linear regulator output becomes active (REG1=5V, REG2=3.3V). Conversely, the status switches off when CTL pin voltage goes lower than 0.8V. The switching regulator doesn't become active when the status of CTL pin is low, if the status of EN pin is high.
(※CTL pin is connected to VIN pin with 1MΩ resistor(pull up) internal IC)

・EN1, 2 (21 pin, 4 pin)
When EN pin voltage is at least 2.3V, the status of the switching regulator becomes active. Conversely, the status switches off when EN pin voltage goes lower than 0.8V.
(※EN pin is connected to AGND pin with 1MΩ resistor(pull down) internal IC)

・REG1 (29 pin)
This is the output pin for 5V linear regulator and also active in power supply for driver and control circuit of the inside. The standby function for REG1 is determined by CTL pin. The voltage is 5V, with 100mA current ability. It is recommended that a 10μF capacitor (X5R or X7R) be established between REG1 and GND.

・REG2 (28 pin)
This is the output pin for 3.3V linear regulator. The standby function for REG2 is determined by CTL. The voltage is 3.3V, with 50mA current ability. It is recommended that a 10μF capacitor (X5R or X7R) be established between REG2 and GND.

・REF (12 pin)
This is the setting pin for output voltage of switching regulator. This IC controls the voltage in the status of REF≒FB.

・FB 1, 2 (14 pin, 11 pin)
This is the feedback pin from the output of switching regulator. This IC controls the voltage in the status of REF≒FB.

・Vo1 (27 pin)
This is the output discharge pin, and output voltage feedback pin for frequency setting. When the voltage is beyond 4.4V from the external power supply during operation, it supplies REG1.

・Vo2 (7 pin)
This is the output discharge pin, and output voltage feedback pin for frequency setting.

・SS1, 2 (19 pin, 6 pin)
This is the setting pin for soft start. The rising time is determined by the capacitor connected between SS and GND, and the fixed current inside IC after it is the status of low in standby mode. It controls the output voltage till SS voltage catch up the REF pin to become the SS terminal voltage.

・FS1, 2 (15 pin, 10 pin)
This is the input pin for setting the frequency. It is available to set it in frequency range is 200KHz to 500kHz.

・ILIM1, 2 (17 pin, 8 pin)
BD9528MUV detects voltage differential between SW and PGND, and set OCP. OCP setting current value is determined by the resistance value of ILIM pin. FET of various Ron is available.

・PGOOD 1, 2 (20 pin, 5 pin)
This is the open drain pin for deciding the output of switching regulator.

・MCTL1, 2 (18 pin, 16 pin)
This is the switching shift pin for SLLM (Simple Light Load Mode). MCTL pin is at low level when it goes lower than 0.8V, and at high level when it goes higher than 2.3V.
(※MCTL pin is connected to AGND pin with 500kΩ resistor(pull down) internal IC)

・AGND (13 pin)
This is the ground pin.

・BOOT1, 2 (22 pin, 3 pin)
This is the power supply pin for high side FET driver. The maximum voltage range to GND pin is to 35V, to SW pin is to 7V. In switching operations, the voltage swings from (VIN+REG1) to REG1 by BOOT pin operation.

・HG1, 2 (23 pin, 2 pin)
This is the highside FET gate drive pin. It is operated in switching between BOOT to SW. In case the output MOS is 3ohm /the status of Hi, 2ohm/the status of Low, it is operated hi-side FET gate in high speed.

・SW1, 2 (24 pin, 1 pin)
This is the ground pin for high side FET drive. The maximum voltage range to GND pin is to 30V. Switching operation swings from the status of BOOT to the status of GND.

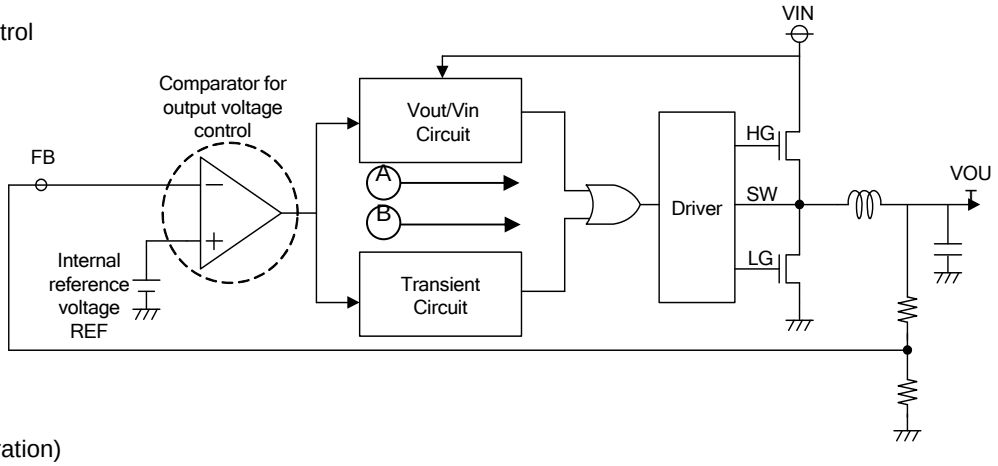
・LG1, 2 (26 pin, 31 pin)
This is the lowside FET gate drive pin. It is operated in switching between REG1 to PGND. In case the output MOS is 2ohm /the status of Hi, 0.5ohm/the status of Low, it is operated low-side FET gate in high speed.

・PGND1, 2 (25 pin, 32 pin)
This is the ground pin for low side FET drive.

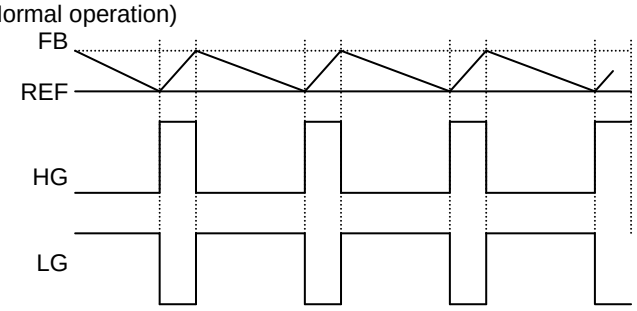
●Explanation of Operation

The BD9528MUV is a 2ch synchronous buck regulator controller incorporating ROHM's proprietary H^3REG CONTROLLA control system. Because controlling of output voltage by a comparator, high response is realized with not relying on the switching frequency. And, when VOUT drops due to a rapid load change, the system quickly restores VOUT by extending the TON time interval. Thus, it serves to improve the regulator's transient response. Activating the Light Load Mode will also exercise Simple Light Load Mode (SLLM) control when the load is light, to further increase efficiency.

H^3Reg^{TM} control



(Normal operation)

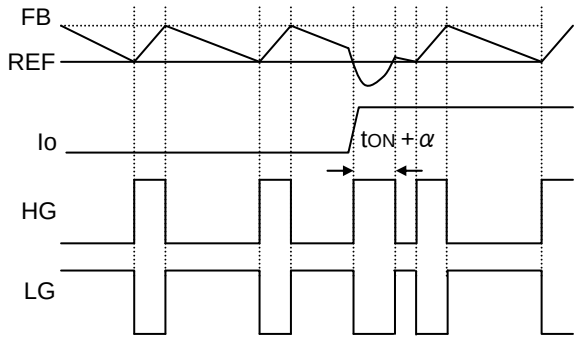


When FB falls to a reference voltage (REF), the drop is detected, activating the H^3REG CONTROLLA system.<Route A>

$$t_{ON} = \frac{VOUT}{VIN} \times \frac{1}{f} \text{ [sec]} \cdot \cdot \cdot (1)$$

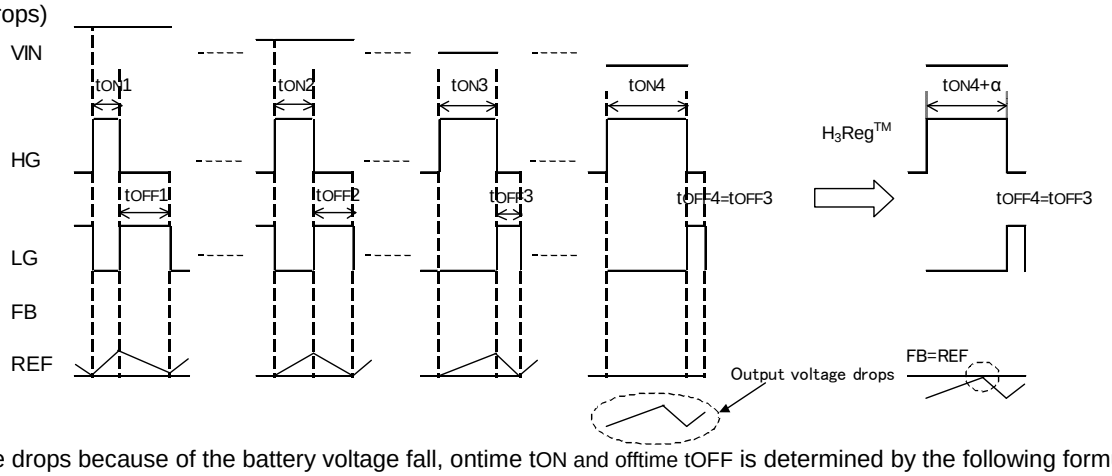
HG output is determined by the formula above.
After the status of HG is OFF, LG go on outputting until output voltage become FB=REF.

(VOUT drops due to a rapid load change)



When VOUT drops due to a rapid load change, and the voltage remains below reference voltage after the programmed tON time interval has elapsed (Output of a comparator for output voltage control =H), the system quickly restores VOUT by extending the tON time, improving the transient response.<Route B> After VOUT restores (FB=REF), HG turns to be OFF, and it goes back to a normal operation.

(when VIN drops)

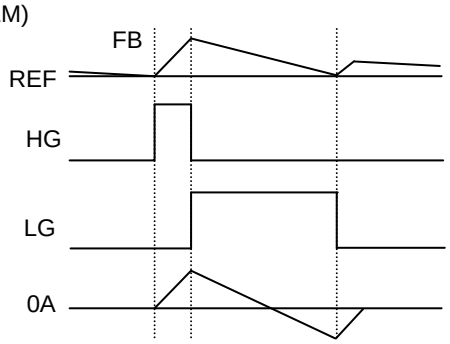


If VIN voltage drops because of the battery voltage fall, ontime tON and offtime tOFF is determined by the following formula: $t_{ON}=VOUT/VIN \times I/f$ and $t_{OFF}=(VIN-VOUT)/VIN \times f$ so that tON lengthen and tOFF shorten to keep output voltage constant. However, if VIN still drops and tOFF equals to tminoff (tminoff : Minimum OFF time, regulated inside IC) , because tOFF cannot shorten any more, as a result output voltage drops. In H^3Reg^{TM} system, lengthening tON time than regulated tON (lengthen tON time until FB＞REF)

enables to operate stable not to drop the output voltage even if VIN turns to be low. With the reason above, it is suitable for 2-cell battery.

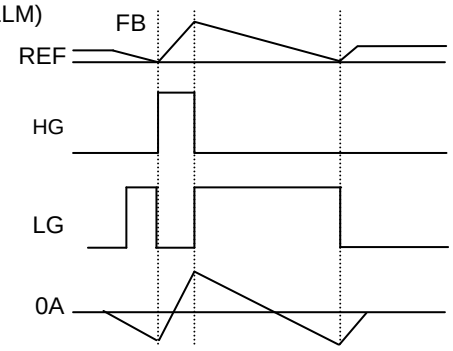
Light Load Control

(SLLM)



In SLLM, when the status of LG is OFF and the coil current is within 0A (it flows to SW from VOUT.), SLLM function is operated to prevent output next HG. The status of HG is ON, when FB falls below reference voltage again.

(QLLM)

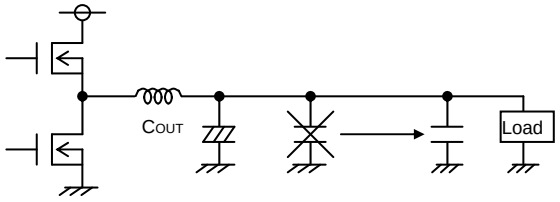


In QLLM, when the status of LG is OFF and the coil current is within 0A (it flows to SW from VOUT.), QLLM function is operated to prevent output next HG.
Then, FB falls below the output programmed voltage within the programmed time (typ=40μs), the status of HG is ON. In case FB doesn't fall in the programmed time, the status of LG is ON forcedly and VOUT falls. As a result, he status of next HG is ON.

MCTL1	MCTL2	Control mode	Running
L	L	SLLM	PWM
L	H	QLLM	PWM
H	X	PWM	PWM

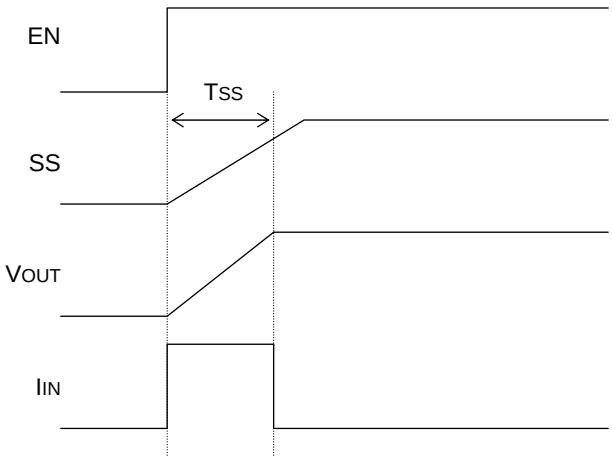
The BD9528MUV operates in PWM mode until SS pin reaches cramp voltage (2.5V), regardless of the control mode setting, in order to operate stable during the operation. .

∗ Attention: H^{3}Reg^{TM}CONTROLLA monitors the supplying current from capacitor to load, using the ESR of output capacitor, and realize the rapid response. Bypass capacitor used at each load (Ex. Ceramic capacitor) exercises the effect with connecting to each load side. Do not put a ceramic capacitor on COUT side of power supply.



● Timing Chart

• Soft Start Function



Soft start is exercised with the EN pin set high. Current control takes effect at startup, enabling a moderate output voltage "ramping start." Soft start timing and incoming current are calculated with formulas (2) and (3) below.

Soft start time

$$Tss = \frac{REF \times Css}{2.3\mu A(typ)} \ [sec] \quad \cdot\cdot\cdot (2)$$

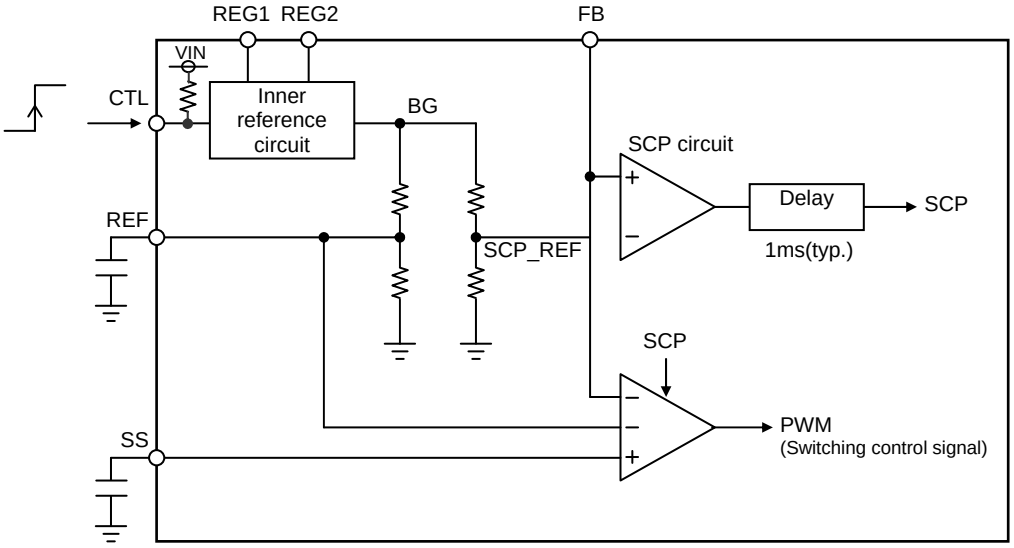
Incoming current

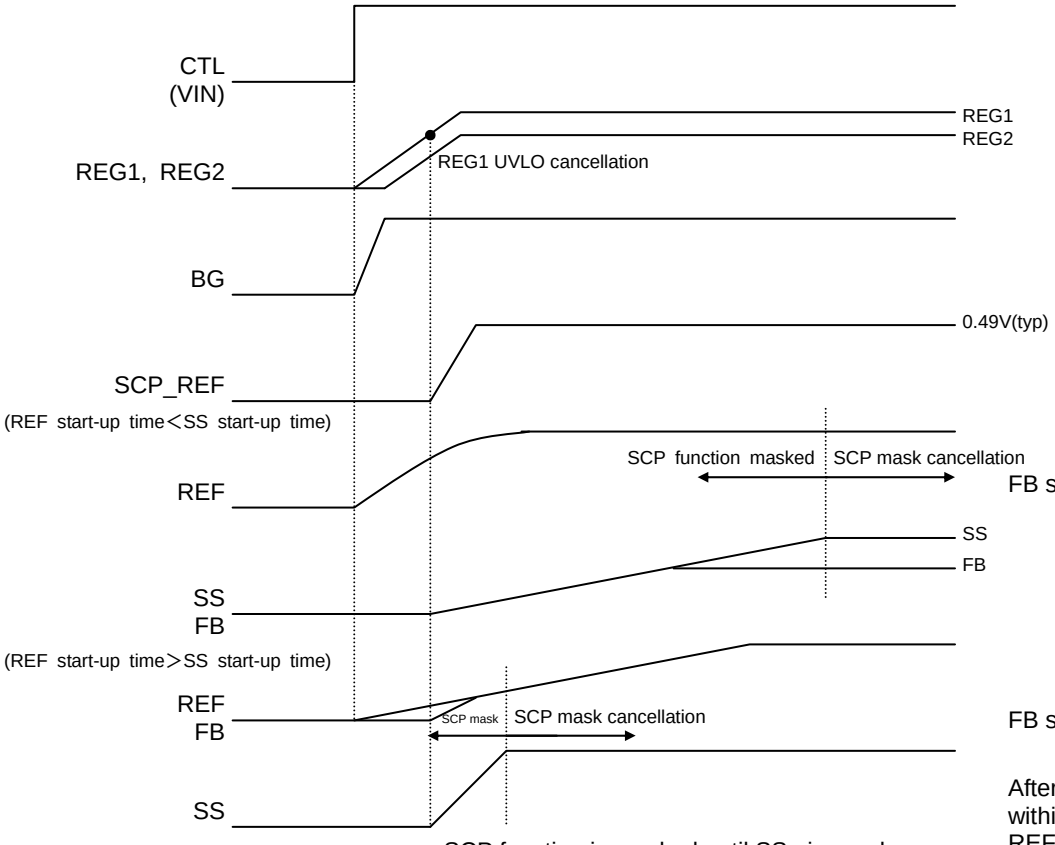
$$I_{IN} = \frac{Co \times V_{OUT}}{Tss} \ [A] \quad \cdot\cdot\cdot (3)$$

(Css: Soft start capacitor; Co: Output capacitor)

Notes when waking up with CTL pin or VIN pin

If EN pin is High or short (or pull up resistor) to REG1 pin, IC starts up by switching CTL pin, the IC might fail to start up (SCP function) with the reason below, please be careful of SS pin and REF pin capacitor capacity.





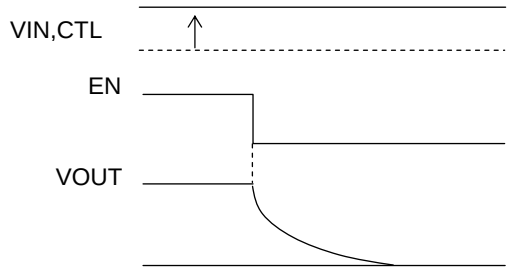
FB starts up as SS reference

FB starts up as REF reference

After the end of SS wake-up, within SCP delay time (1ms), if REF voltage does not reach SCP_REF(0.49V), SCP turns ON and shut down.

SCP function is masked until SS pin reaches cramp voltage (2.5V).

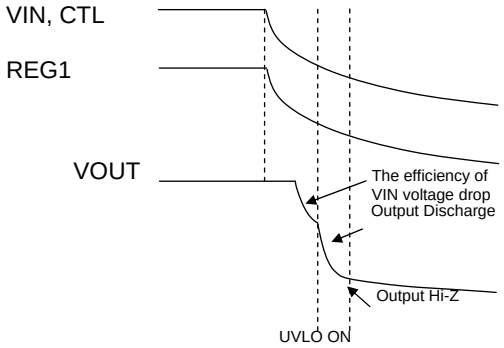
●Output Discharge



It will be available to use if connecting VOUT pin to DC/DC output. (Total about 100Ω) . Discharge function operates when ①EN='L' ②UVLO=ON(If input voltage is low) ③SCP Latch time ④TSD=ON. The function at output discharge time is shown as left.

(1)during EN='H'→ 'L'

If EN pin voltage is below than EN threshold voltage, output discharge function is operated, and discharge output capacitor charge.



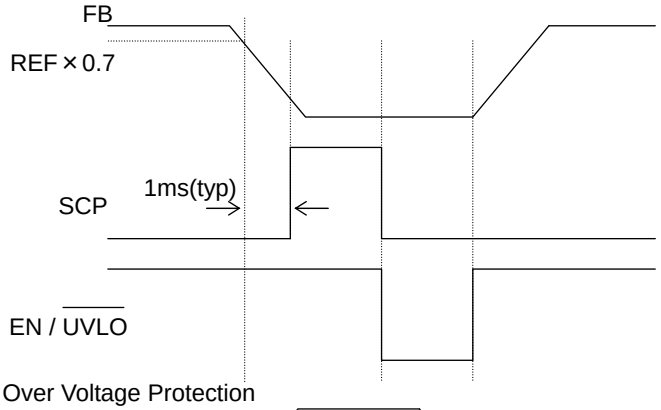
(2) during VIIN=CTL=H→0V

① IC is in normal operation until REG1 voltage becomes lower than UVLO voltage. However, because VIN voltage also becomes low, output voltage will drop, too.

② If REG1 voltage reaches the UVLO voltage, output discharge function is operated, and discharge output capacitor charge.

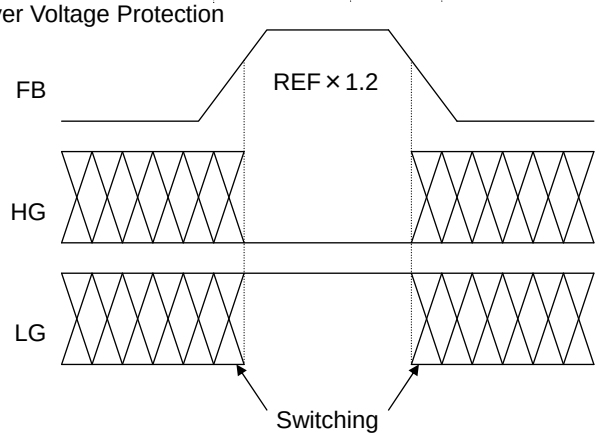
③ In addition, if REG1 voltage drops, inner IC logic cannot operate, so that output discharge function does not work, and becomes output Hi-z. （In case, FB has resistor against GND, discharge at the resistor.）

・Timer Latch Type Short Circuit Protection



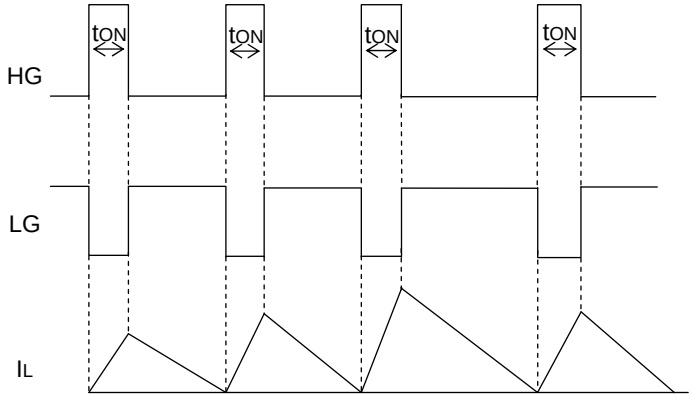
Short protection kicks in when output falls to or below REF X 0.7.
When the programmed time period elapses, output is latched OFF to prevent destruction of the IC. (HG=Low, LG=Low) Output voltage can be restored either by reconnecting the EN pin or disabling UVLO.

・Over Voltage Protection



When output rise to or above REF × 1.2 (typ), output over voltage protection is exercised, and low side FET goes up maximum for reducing output.(LG=High, HG=Low).When output falls, output voltage can be restored., and go back to the normal operation.

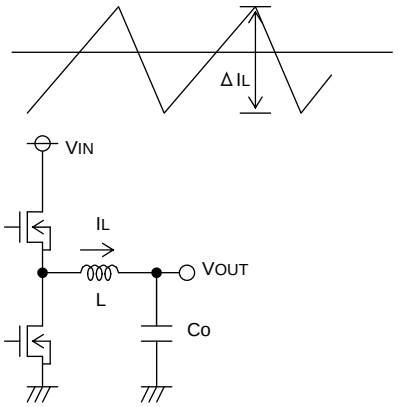
・Over current protection circuit



During the normal operation, when FB becomes less than REF, HG becomes High during the time t_{ON}, and after HG becomes OFF, it output LG.
However, when inductor current exceeds I_{LIMIT} threshold, next HG pulse doesn't pulsate until it is lower than I_{LIMIT} level.

● External Component Selection

1. Inductor (L) selection



Output ripple current

The inductor value is a major influence on the output ripple current. As formula (4) below indicates, the greater the inductor or the switching frequency, the lower the ripple current.

$$\Delta I_L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \quad [A] \cdots (4)$$

The proper output ripple current setting is about 30% of maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT}max. \quad [A] \cdots (5)$$

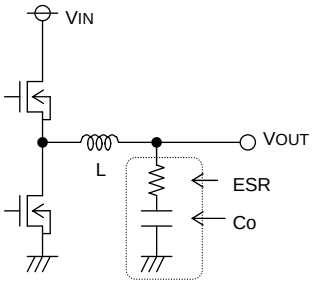
$$L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f} \quad [H] \cdots (6)$$

(ΔI_L: output ripple current; f: switch frequency)

※Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. In selecting the inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor rated current value.

※To minimize possible inductor damage and maximize efficiency, choose a inductor with a low (DCR, ACR) resistance.

2.Output Capacitor (C_O) Selection



Output Capacitor

When determining the proper output capacitor, be sure to factor in the equivalent series resistance required to smooth out ripple volume and maintain a stable output voltage range.

Output ripple voltage is determined as in formula (7) below.

$$\Delta VOUT = \Delta IL \times ESR + ESL \times \Delta IL/T_{ON} \cdots (7)$$

(ΔI_L: Output ripple current; ESR: C_O equivalent series resistance)

※ In selecting a capacitor, make sure the capacitor rating allows sufficient margin relative to output voltage. Note that a lower ESR can minimize output ripple voltage.

Please give due consideration to the conditions in formula (8) below for output capacity, bear in mind that output rise time must be established within the soft start time frame. Capacitor for bypass capacitor is connected to Load side which connect to output in output capacitor capacity ($C_{EXT,}$ figure above). Please set the soft start time or over current detecting value, regarding these capacities.

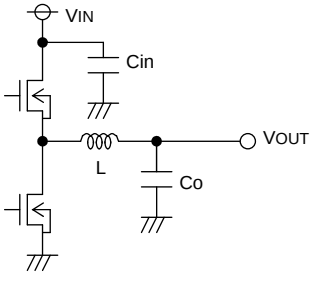
$$Co \leqq \frac{Tss \times (Limit - I_{OUT})}{V_{OUT}} \quad \cdots (8)$$

Tss: Soft start time

Limit: Over current detection

Note: Improper capacitor may cause startup malfunctions.

3. Input Capacitor (Cin) Selection



Input Capacitor

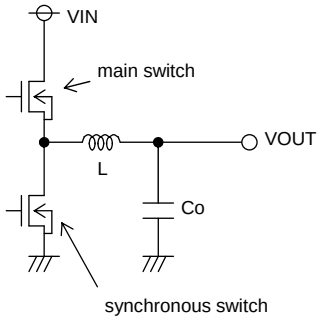
The input capacitor selected must have low enough ESR resistance to fully support large ripple output, in order to prevent extreme over current. The formula for ripple current IRMS is given in (9) below.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{IN}(V_{IN}-V_{OUT})}}{VIN} \quad [A] \cdots (9)$$

Where $V_{IN} = 2 \times V_{OUT}$, $IRMS = \frac{I_{OUT}}{2}$

A low ESR capacitor is recommended to reduce ESR loss and maximize efficiency.

4. MOSFET Selection



MOSFET may cause the loss as below, so please select proper FET for each.

＜Loss on the main MOSFET＞

$$Pmain=P_{RON}+P_{GATE}+P_{TRAN}$$

$$= \frac{V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + Ciss \times f \times V_{DD} + \frac{V_{IN}^2 \times Crss \times I_{OUT} \times f}{I_{DRIVE}} \quad \cdots (10)$$

(Ron: On-resistance of FET; Ciss: FET gate capacitance;
f: Switching frequency Crss: FET inverse transfer function;
I_{DRIVE}: Gate peak current)

＜Loss on the synchronous MOSFET＞

$$Psyn=P_{RON}+P_{GATE}$$

$$= \frac{V_{IN}-V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + Ciss \times f \times V_{DD} \quad \cdots (11)$$

5. Setting output voltage

This IC is operated that output voltage is REF≒FB.
And it is operated that output voltage is feed back to FB pin.

<Output Voltage>

$$V_{OUT} = \frac{(R1 + R2)}{R2} \times REF(0.7V) + \frac{1}{2}\Delta V_{OUT}$$

(ΔVOUT:Output ripple voltage)

$$\Delta V_{OUT} = \Delta I_{Ripple} \times ESR$$

(ΔIripple: ripple current of coil, ESR: ESR of output capacitor)

$$\Delta I_{Ripple} = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{(L \times V_{IN} \times f)}$$

(L:inductance[H] f:switching frequency[Hz])

※(Notice) Please set ΔVOUT more than 20mV

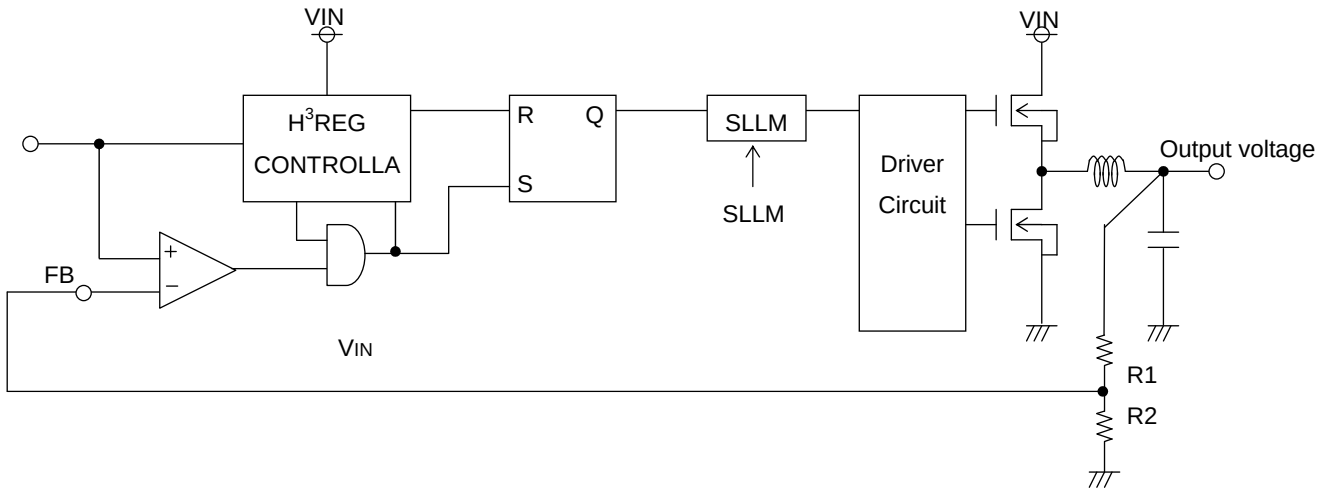
Ex. VIN=20V,VOUT=5V,f=300kHz,L=2.5uH,ESR=20mΩ,R1=56KΩ,R2=9.1kΩ

ΔIripple=(20V-5V)×5V/(2.5×10^{-6}H×20V×300×10^{3}Hz)=5[A]

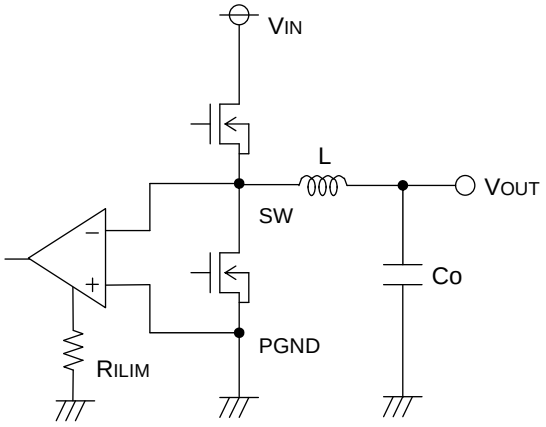
ΔVOUT=5A×20×10^{-3}Ω=0.1[V]

VOUT=(51kΩ+9.1kΩ)/9.1kΩ+1/2×0.1V=5.057[V]

Select (R1 + R2) under 100KΩ(recommend)



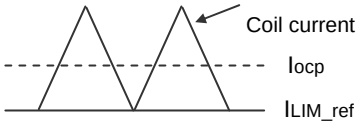
6. Setting over current protection



Detecting the ON resistance (between SW and PGND voltage) of MOSFET at low side, it set the over current voltage protection.
Over current reference voltage (I_{LIM_ref}) is determined as in formula(12) below.

$$I_{LIM\_REF} = \frac{10 \times 10^3}{R_{ILIM}[k\Omega] \times RON[m\Omega]} \quad [A] \cdots (12)$$

(R_{ILIM}: Resistance for setting of over current voltage protection value[kΩ]
RON: Low side ON resistance value of FET[mΩ])



However, the value, which set the over current protection actually, is determined by the formula (13) below.

$$I_{ocp} = I_{LIM\_ref} + \frac{1}{2}\Delta I_L$$

$$= I_{LIM\_ref} + \frac{1}{2} \times \frac{VIN - Vo}{L} \times \frac{1}{f} \times \frac{Vo}{VIN} \cdots (13)$$

(ΔIL：Coil ripple current[A], VIN：Input voltage[V], Vo：Output voltage[V]
f ：Switching frequency[HZ], L：Coil inductance[H])

(Example)

If load current 5A want to be realized with VIN=6～19V, VOUT=5V, f =400kHz, L=2.5uH, RON=20mΩ, the formula would be below.

$$I_{ocp} = \frac{10k}{R_{ILIM}[k\Omega] \times R_{ON}[m\Omega]} + \frac{1}{2} \times \frac{VIN - Vo}{L} \times \frac{1}{f} \times \frac{Vo}{VIN} > 5$$

When VIN=6V, Iocp will be minimum(this is because the ripple current is also minimum) so that if each condition is input, the formula will be the following: $R_{ILIM} < 109.1[k\Omega]$.

※To design the actual board, please consider enough margin for FET ON resistor dispersion, Coil inductor dispersion, IC over current reference value dispersion, frequency dispersion.

7. Relation between output voltage and TON time

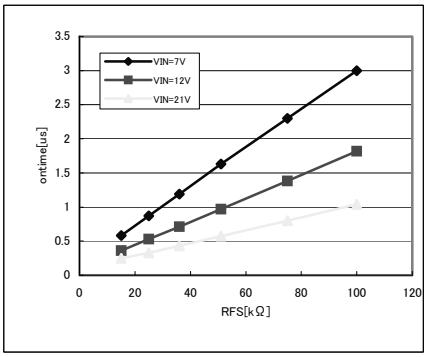
The BD9528MUV, both 1ch and 2ch, are high efficiency synchronous regulator controller with frequency variable.
TON time varies with Input voltage [VIN], output voltage [VOUT], and RFS of FS pin resistance.
TON time is calculated with the following formula:

$$T_{ON} = k \frac{VOUT \cdot RFS}{VIN} \quad [nsec] \cdots (14)$$

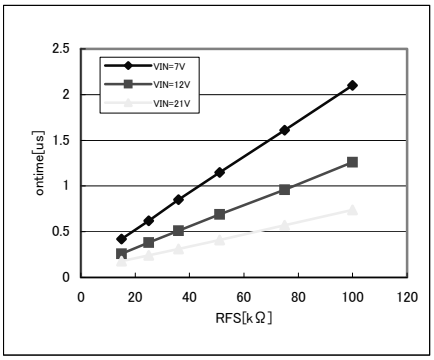
From TON time above, frequency on application condition is following:

$$Frequency = \frac{VOUT}{VIN} \times \frac{1}{Ton} \quad [kHz] \cdots (15)$$

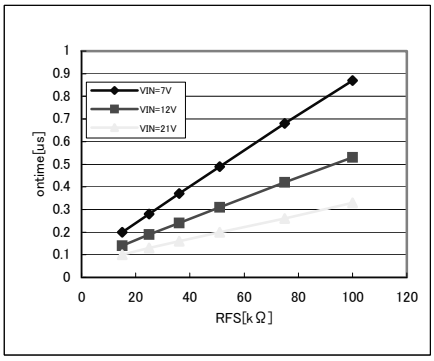
However, real-life considerations (such as the external MOSFET gate capacitor and switching speed) must be factored in as they affect the overall switching rise and fall time, so please confirm in reality by the instrument.



RFS – ontime(VOUT=5V)



RFS – ontime(VOUT=3.3V)



RFS – ontime(VOUT=1V)

8. Relation between output voltage and frequency

Because the BD9528MUV is TON time focused regulator controller, if output current is up, switching loss of Coil, MOSFET and output capacitor will increase, and frequency will be fast.
Loss of each Coil, MOSFET and output capacitor are below.

① Coil loss $= IOUT^2 \times DCR$

② MOSFET(High Side) loss $= IOUT^2 \times Ronh \times \frac{VOUT}{VIN}$

③ MOSFET(Low Side) loss $= IOUT^2 \times Ronl \times \left(1- \frac{VOUT}{VIN}\right)$

(Ronh : ON resistance of high side MOSFET, Ronl : ON resistance of low side MOSFET,
ESR : Output capacitor equivalent cascade resistance)

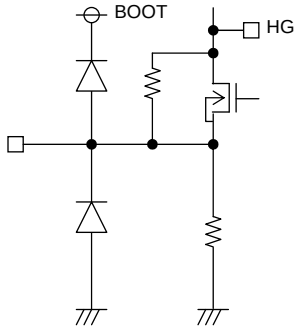
Regarding those loss above and frequency formula, it is determined below.

$$T\ (=1/Freq) = \frac{VIN \times IOUT \times TON}{VOUT \times IOUT + ① + ② + ③} \cdot\cdot\cdot (16)$$

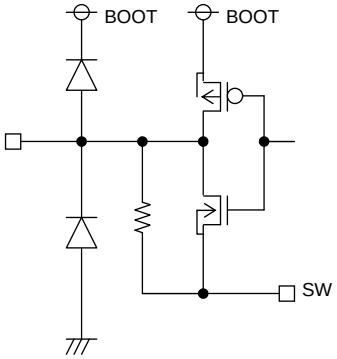
However, real-life considerations (such as parasitic resistance element of Layout pattern) must be factored in as they affect the loss, please confirm in reality by the instrument.

●I/O Equivalent Circuit

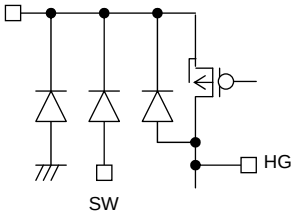
1, 24pin (SW2, SW1)



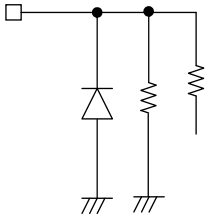
2, 23pin (HG2, HG1)



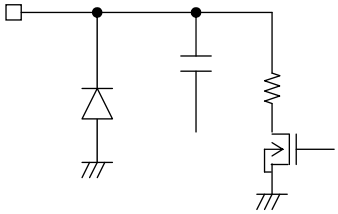
3, 22pin (BOOT2, BOOT1)



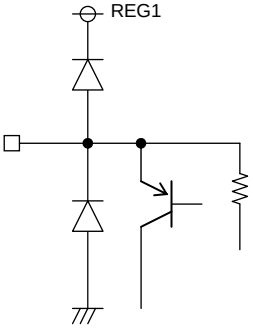
4, 21pin (EN2, EN1)



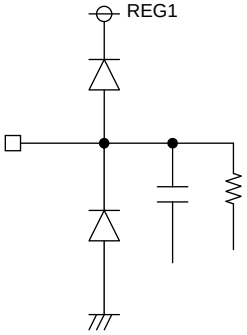
5, 20pin (PGOOD2, PGOOD1)



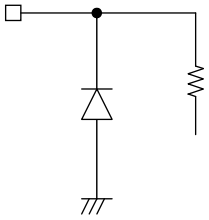
6, 19pin (SS2, SS1)



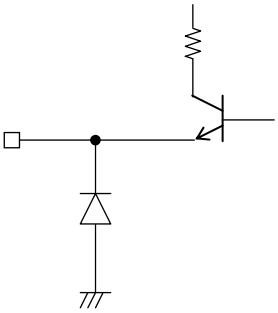
12pin (REF)



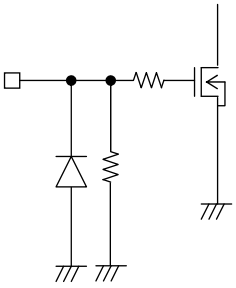
11, 14pin (FB2, FB1)



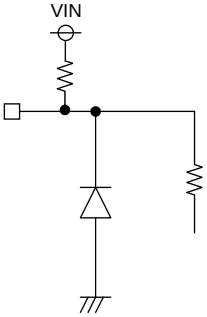
10, 15pin (FS2, FS1)



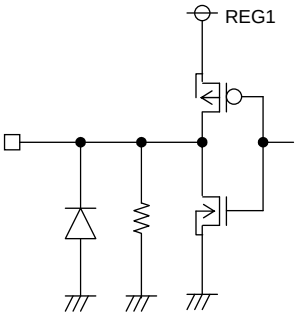
16, 18pin (MCTL2, MCTL1)



9pin (CTL)

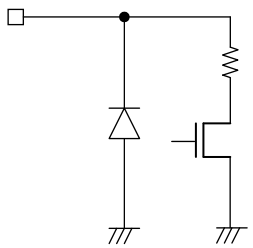


26, 31pin (LG1, LG2)

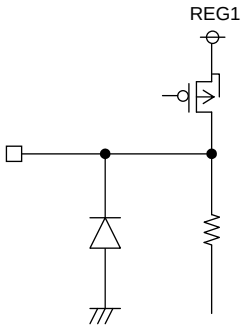


●I/O Equivalent Circuit

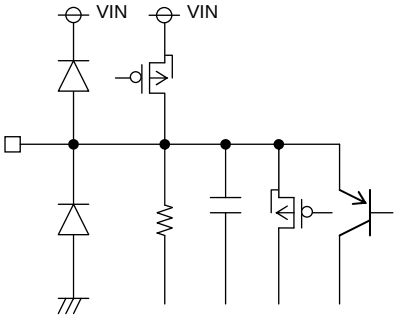
7, 27pin (Vo2, Vo1)



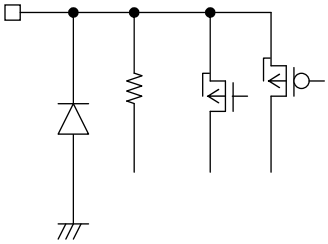
28pin (REG2)



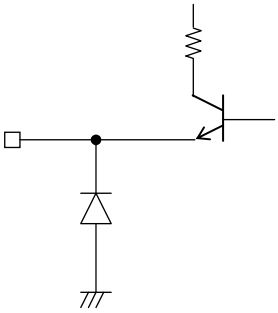
29pin (REG1)



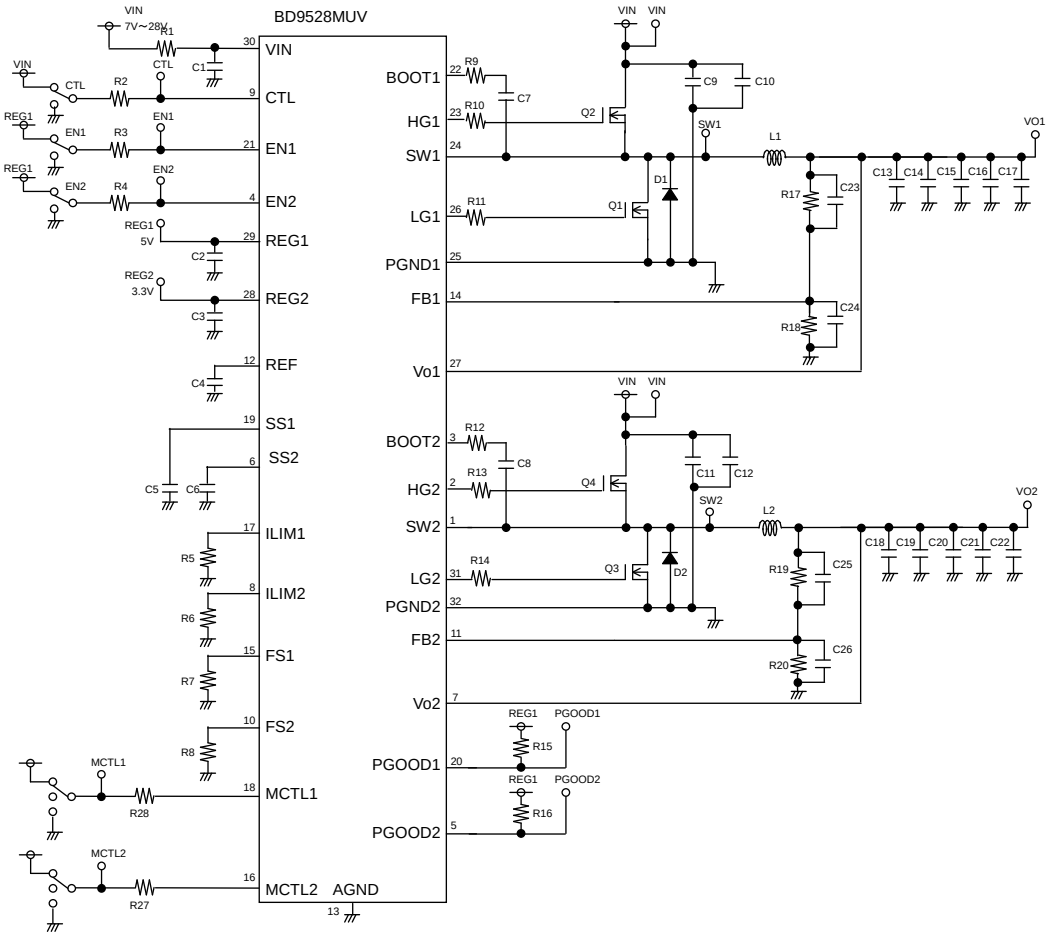
30pin (VIN)



8, 17pin (ILIM2, ILIM1)



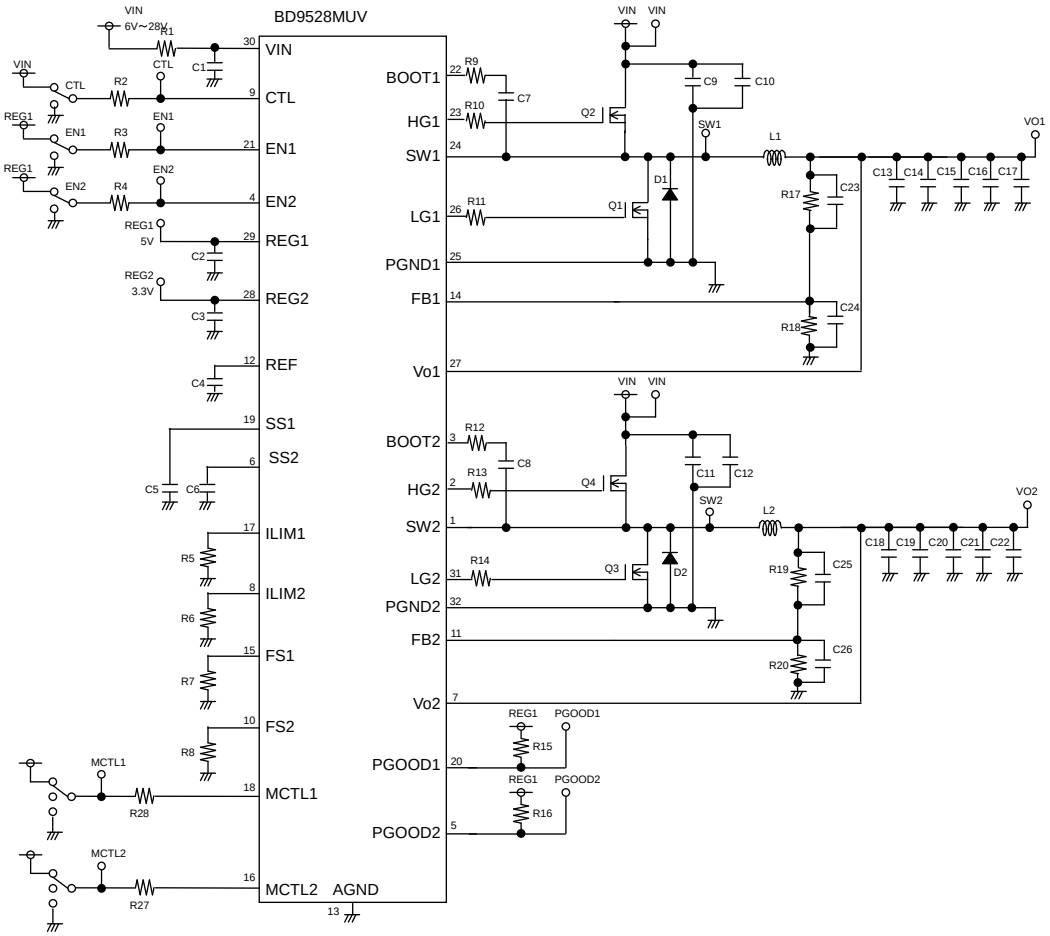
●**Evaluation Board Circuit** (Vo1=5V/8A f1=300kHz Vo2=3.3V/8A f2=300kHz)



DESIGNATION	RATING	PART No.	COMPANY
R1	0Ω	-	-
R2	-	-	-
R3	0Ω	-	-
R4	0Ω	-	-
R5	68kΩ	MCR03	ROHM
R6	68kΩ	MCR03	ROHM
R7	75kΩ	MCR03	ROHM
R8	75kΩ	MCR03	ROHM
R9	0Ω	-	-
R10	0Ω	-	-
R11	0Ω	-	-
R12	0Ω	-	-
R13	0Ω	-	-
R14	0Ω	-	-
R15	100kΩ	MCR03	ROHM
R16	100kΩ	MCR03	ROHM
R17	91kΩ	MCR03	ROHM
R18	15kΩ	MCR03	ROHM
R19	30kΩ	MCR03	ROHM
R20	8.2kΩ	MCR03	ROHM
R27	0Ω	-	-
R28	0Ω	-	-
C1	10uF(25V)	CM32X7R106M25A	KYOCERA
C2	10uF(6.3V)	GRM21BB10J106KD	MURATA
C3	10uF(6.3V)	GRM21BB10J106KD	MURATA
C4	0.1uF(6.3V)	GRM21BB10J104KD	MURATA
C5	2200pF(50V)	GRM188B11H102KD	MURATA
C6	2200pF(50V)	GRM188B11H102KD	MURATA

DESIGNATION	RATING	PART No.	COMPANY
C7	0.47uF(10V)	GRM188B11A474KD	MURATA
C8	0.47uF(10V)	GRM188B11A474KD	MURATA
C9	10uF(25V)	CM32XR7106M25A	KYOCERA
C10	-	-	-
C11	10uF(25V)	CM32XR7106M25A	KYOCERA
C12	-	-	-
C13	330uF	6TPE330MI	SANYO
C14	-	-	-
C15	-	-	-
C16	-	-	-
C17	-	-	-
C18	330uF	6TPE330MI	SANYO
C19	-	-	-
C20	-	-	-
C21	-	-	-
C22	-	-	-
C23	-	-	-
C24	-	-	-
C25	-	-	-
C26	-	-	-
D1	Diode	RSX501L-20	ROHM
D2	Diode	RSX501L-20	ROHM
L1	2.5uH	CDEP105NP-2R5MC-32	Sumida
L2	2.5uH	CDEP105NP-2R5MC-32	Sumida
Q1	FET	uPA2709	NEC
Q2	FET	uPA2709	NEC
Q3	FET	uPA2709	NEC
Q4	FET	uPA2709	NEC
U1	-	BD9528MUV	ROHM

●**Evaluation Board Circuit for Low input voltage**(Vo1=5V/8A f1=300kHz Vo2=3.3V/8A f2=300kHz)



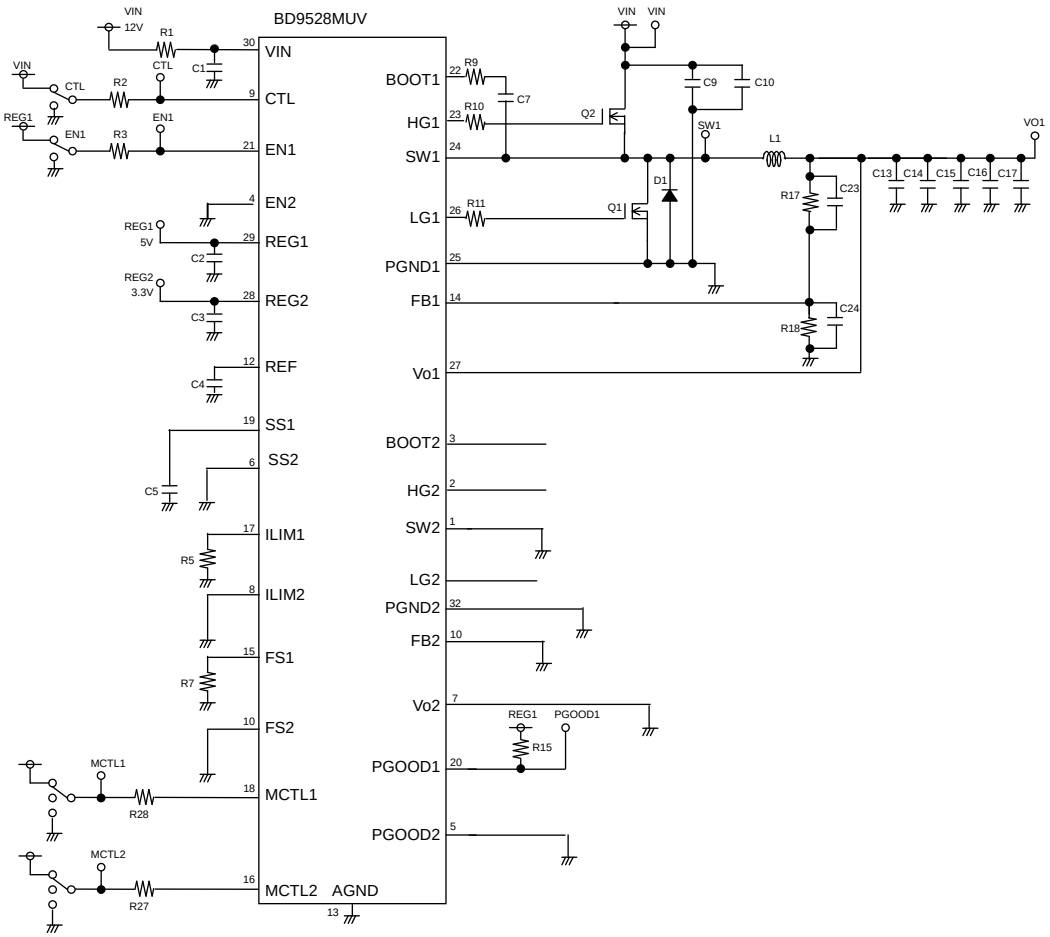
DESIGNATION	RATING	PART No.	COMPANY
R1	0Ω	-	-
R2	-	-	-
R3	0Ω	-	-
R4	0Ω	-	-
R5	68kΩ	MCR03	ROHM
R6	68kΩ	MCR03	ROHM
R7	75kΩ	MCR03	ROHM
R8	75kΩ	MCR03	ROHM
R9	0Ω	-	-
R10	10Ω	-	-
R11	10Ω	-	-
R12	0Ω	-	-
R13	10Ω	-	-
R14	10Ω	-	-
R15	100kΩ	MCR03	ROHM
R16	100kΩ	MCR03	ROHM
R17	56kΩ	MCR03	ROHM
R18	9.1kΩ	MCR03	ROHM
R19	30kΩ	MCR03	ROHM
R20	8.2kΩ	MCR03	ROHM
R27	0Ω	-	-
R28	0Ω	-	-
C1	10uF(25V)	CM32X7R106M25A	KYOCERA
C2	10uF(6.3V)	GRM21BB10J106KD	MURATA
C3	10uF(6.3V)	GRM21BB10J106KD	MURATA
C4	0.1uF(6.3V)	GRM21BB10J104KD	MURATA
C5	2200pF(50V)	GRM188B11H102KD	MURATA
C6	2200pF(50V)	GRM188B11H102KD	MURATA

DESIGNATION	RATING	PART No.	COMPANY
C7	0.47uF(10V)	GRM188B11A474KD	MURATA
C8	0.47uF(10V)	GRM188B11A474KD	MURATA
C9	10uF(25V)	CM32XR7106M25A	KYOCERA
C10	-	-	-
C11	10uF(25V)	CM32XR7106M25A	KYOCERA
C12	-	-	-
C13	330uF	6TPB330ML	SANYO
C14	-	-	-
C15	-	-	-
C16	-	-	-
C17	-	-	-
C18	330uF	6TPE330MI	SANYO
C19	-	-	-
C20	-	-	-
C21	-	-	-
C22	-	-	-
C23	10pF(50V)	-	-
C24	-	-	-
C25	-	-	-
C26	-	-	-
D1	Diode	RSX501L-20	ROHM
D2	Diode	RSX501L-20	ROHM
L1	2.5uH	CDEP105NP-2R5MC-32	Sumida
L2	2.5uH	CDEP105NP-2R5MC-32	Sumida
Q1	FET	uPA2709	NEC
Q2	FET	uPA2709	NEC
Q3	FET	uPA2709	NEC
Q4	FET	uPA2709	NEC
U1	-	BD9528MUV	ROHM

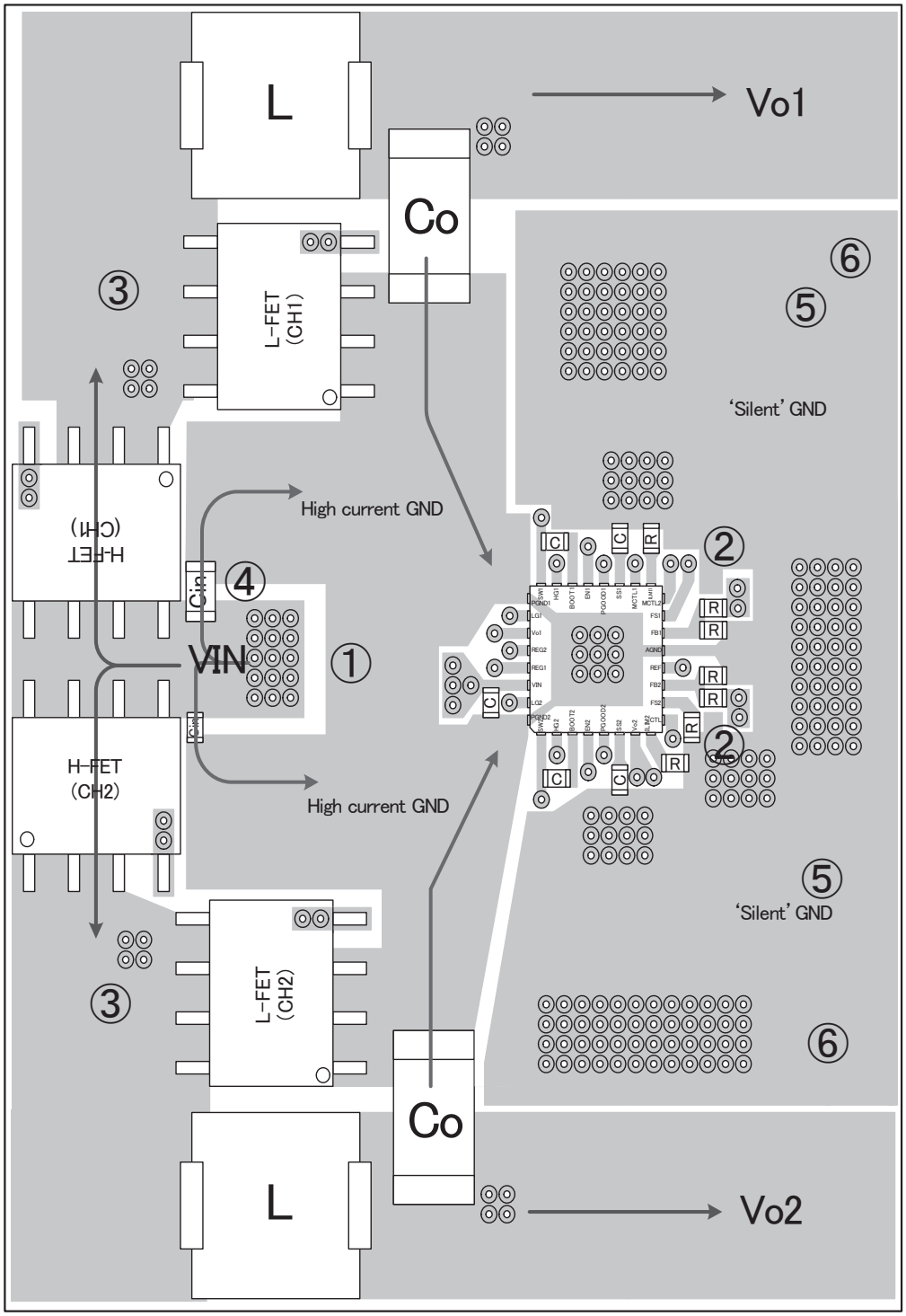
●Handling method of unused pin during using only DC/DC 1ch

If using only 1ch DC/DC and 2ch pin is set to be off at all times, please manage the unused pin as diagram below.

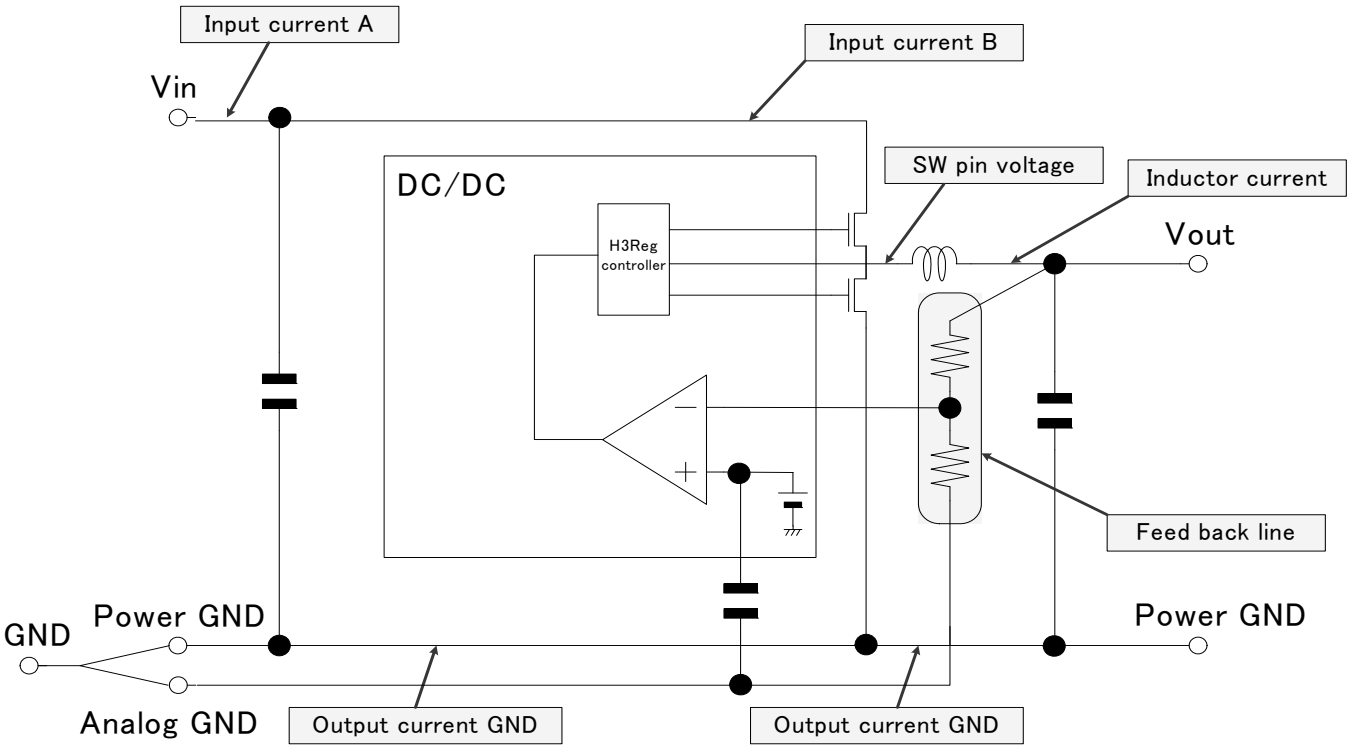
PIN No,	PIN name	Management
1	SW2	GND
2	HG2	Open
3	BOOT2	Open
4	EN2	GND
5	PGOOD2	GND
6	SS2	GND
7	Vo2	GND
8	ILIM1	GND
10	FB2	GND
11	FS2	GND
31	LG2	Open

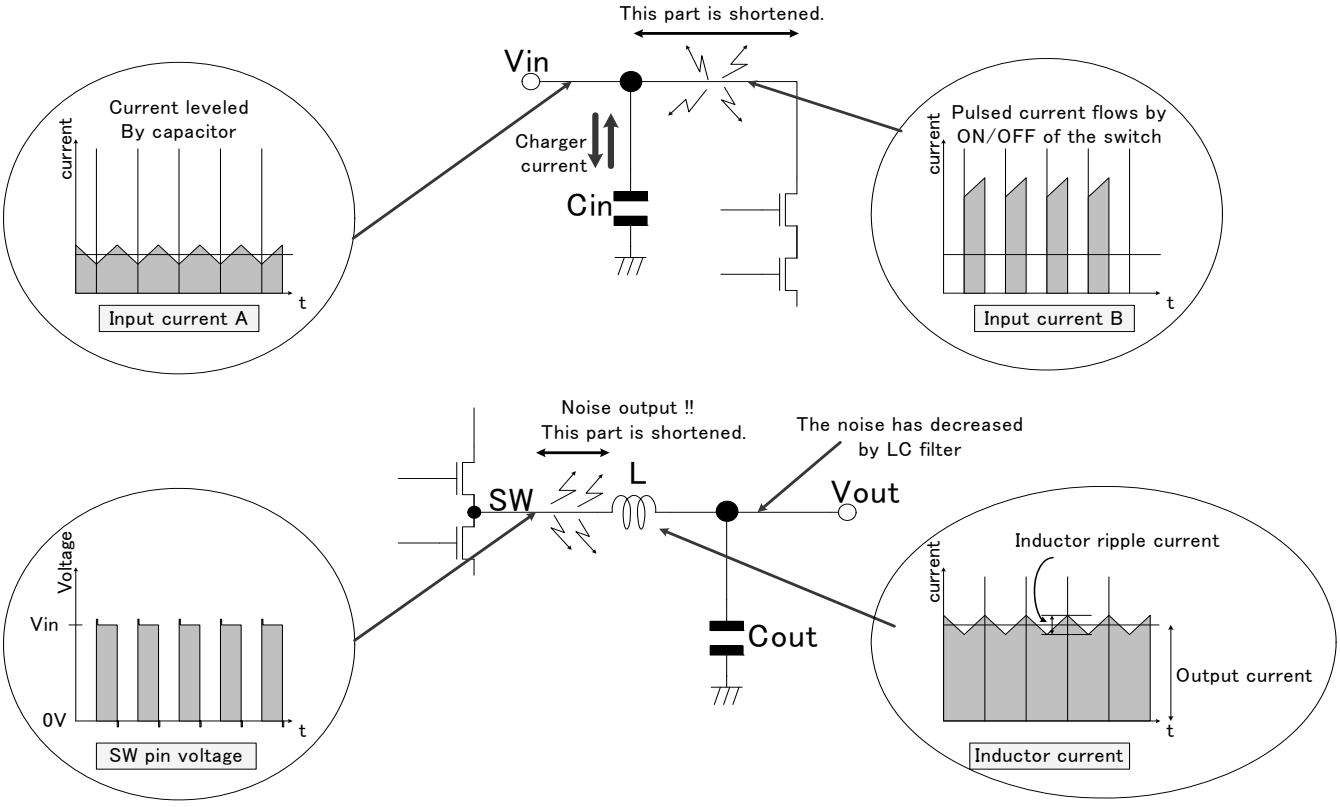


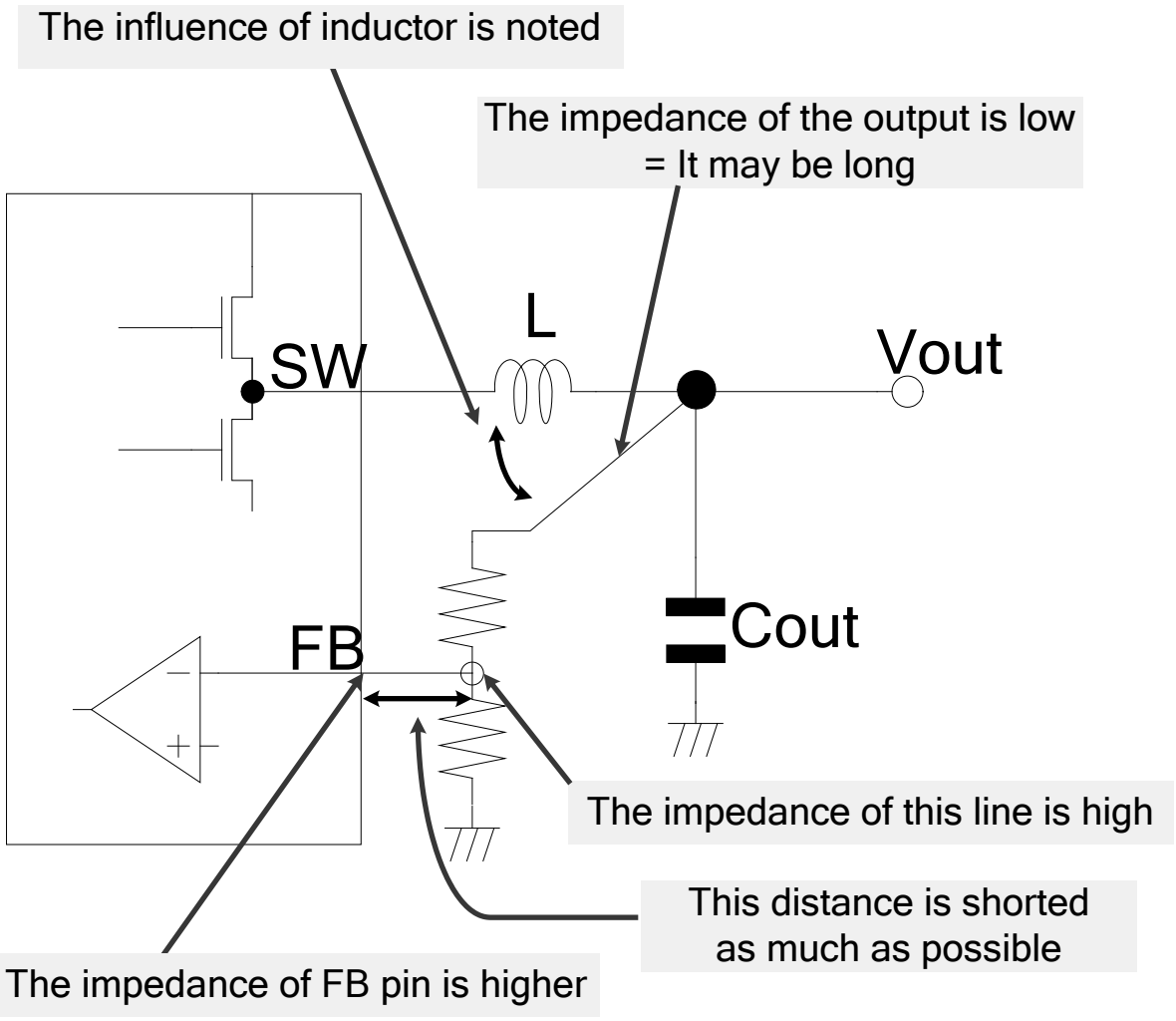
●**Example of PCB layout**

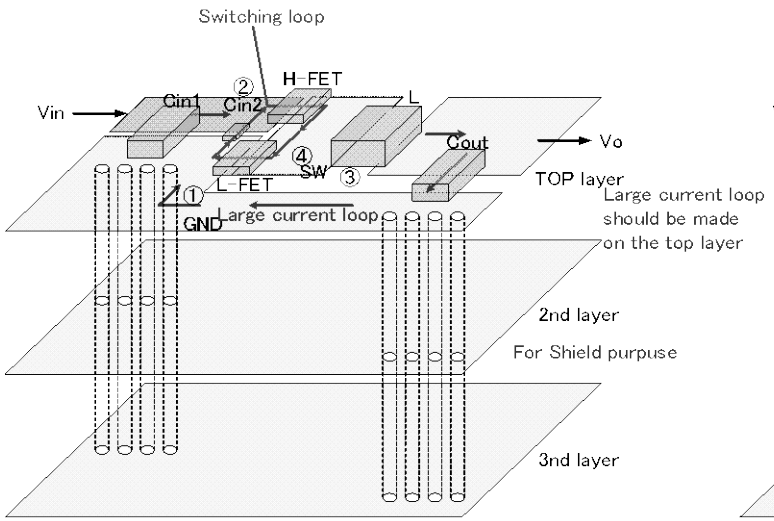


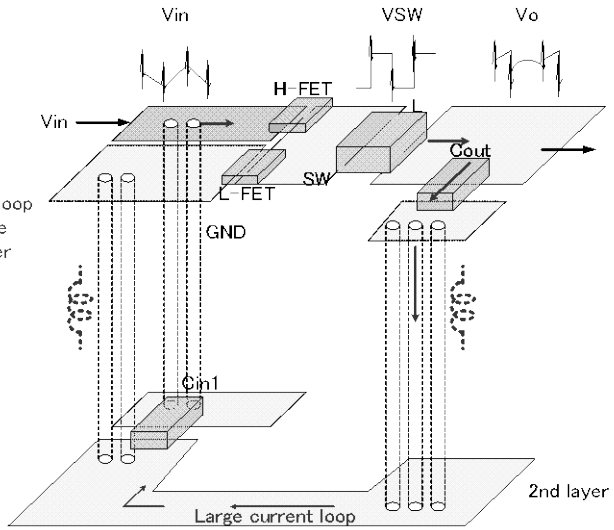
①Because high pulse current rush into power loop, consisted of input capacitor Cin, Output inductor L, and Output capacitor Co, this part layout should be built, including GND pattern, at parts side (upper side). Also ,please avoid to draw via formation in power loop line. (The reason is that it will be a factor of noise because via oneself holds some nH parasitic inductance)
②FB pin has comparatively high impedance, so floating capacity should be minimum as possible. And feedback wiring from output should be taken properly, and put on shield, not going through around L (because of magnetic). Please be careful in drawing)
③Trace from SW node pin to inductor should be cut short . And both inductor element pattern should be kept away. (Closer wiring has SW node noise influence Vo by parasitic capacity between wiring). This layout example shows that SW node is outside, but if the application board will be like that , SW node should be shielding, and consider the influence to other circuit.
④Input capacitor Cin should be placed cloase to IC with low inductance and low impedance . If that is difficult, please place a capacitor for high frequency removal with PKG size small like 0.1uF (ESL small).
⑤2 layer and 3 layer are plain GND, so connect from parts side GND to plain GND by low impedance with many via as possible. Inner GND is only for shielding, so that not to form loop for high current .
⑥Please take GND pattern space widely, and design layout to be able to increase radiation efficiency.
⑦FS pin nad ILIM pin has high impedance. External resistor should be connected to "Silent GND".











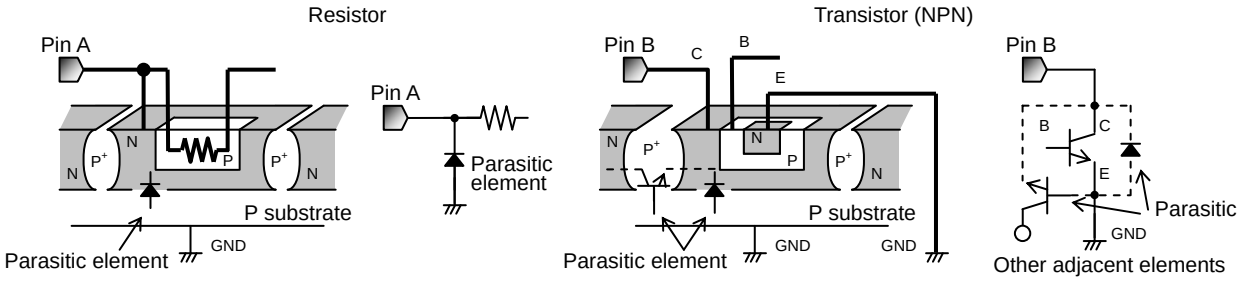
Good layout

Bad layout

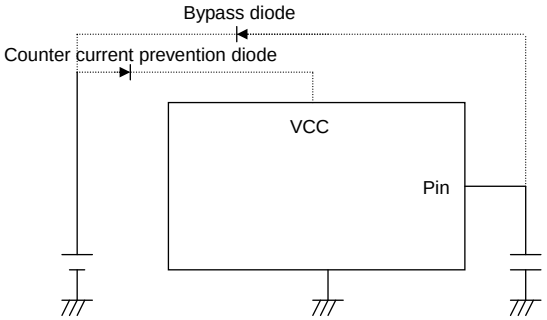
●Notes for use

1. This integrated circuit is a monolithic IC, which (as shown in the figure below), has P^+ isolation in the P substrate and between the various pins. A P-N junction is formed from this P layer and N layer of each pin, with the type of junction depending on the relation between each potential, as follows:
   - When GND＞ element A＞ element B, the P-N junction is a diode.
   - When element B＞GND element A, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, as well as operating malfunctions and physical damage. Therefore, be careful to avoid methods by which parasitic diodes operate, such as applying a voltage lower than the GND (P substrate) voltage to an input pin.



2. In some modes of operation, power supply voltage and pin voltage are reversed, giving rise to possible internal circuit damage. For example, when the external capacitor is charged, the electric charge can cause a VCC short circuit to the GND. In order to avoid these problems, inserting a VCC series countercurrent prevention diode or bypass diode between the various pins and the VCC is recommended.



3. Absolute maximum rating

   Although the quality of this IC is rigorously controlled, the IC may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because short mode or open mode cannot be specified when the IC is destroyed, it is important to take physical safety measures such as fusing if a special mode in excess of absolute rating limits is to be implemented.

4.GND potential

Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode.

5. Thermal design

In order to build sufficient margin into the thermal design, give proper consideration to the allowable loss (Power Dissipation) in actual operation.

6. Short-circuits between pins and incorrect mounting position

When mounting the IC onto the circuit board, be extremely careful about the orientation and position of the IC. The IC may be destroyed if it is incorrectly positioned for mounting. Do not short-circuit between any output pin and supply pin or ground, or between the output pins themselves. Accidental attachment of small objects on these pins will cause shorts and may damage the IC.

7. Operation in strong electromagnetic fields

Use in strong electromagnetic fields may cause malfunctions. Use extreme caution with electromagnetic fields.

8. Thermal shutdown circuit

This IC is provided with a built-in thermal shutdown (TSD) circuit, which is activated when the operating temperature reaches 175℃ (standard value), and has a hysteresis range of -15℃ (standard value). When the IC chip temperature rises to the threshold, all the inputs automatically turn OFF. Note that the TSD circuit is provided for the exclusive purpose shutting down the IC in the presence of extreme heat, and is not designed to protect the IC per se or guarantee performance when or after extreme heat conditions occur. Therefore, do not operate the IC with the expectation of continued use or subsequent operation once the TSD is activated.

9. Capacitor between output and GND

When a larger capacitor is connected between the output and GND, Vcc or VIN shorted with the GND or 0V line – for any reason – may cause the charged capacitor current to flow to the output, possibly destroying the IC. Do not connect a capacitor larger than 1000uF between the output and GND.

10. Precautions for board inspection

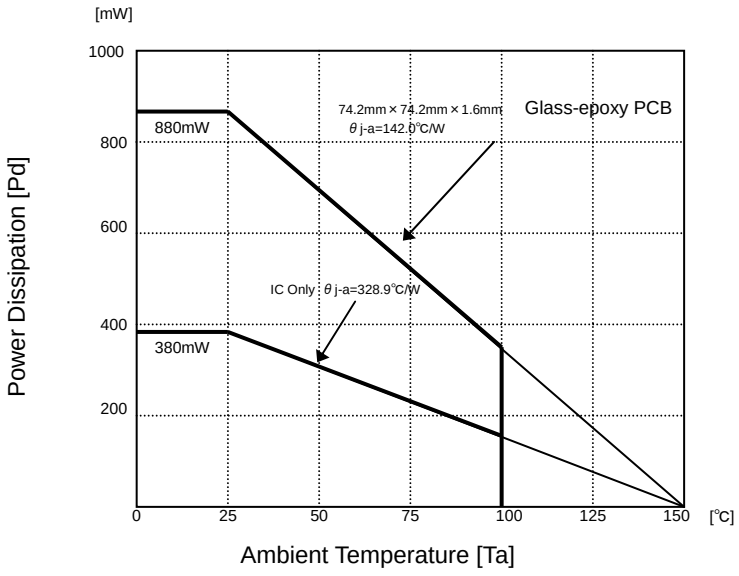
Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC. Therefore, be certain to use proper discharge procedure before each process of the operation. To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handling, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

11. GND wiring pattern

When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

●Thermal Derating Curve

◎ VQFN032V5050



●Ordering part number

B	D	9	5	2	8	M	U	V	-	E	2

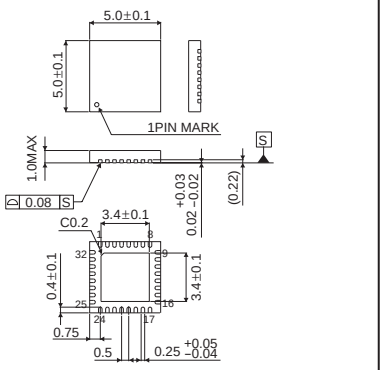
Part No. (BD)

Part No. (9528)

Package
MUV: VQFN032V5050

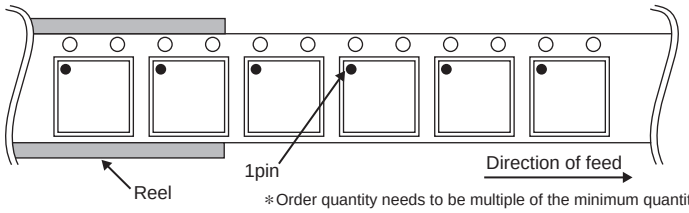
Packaging and forming specification
E2: Embossed tape and reel

VQFN032V5050



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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